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Technical Committee

ATM-MPLS Network Interworking Version 1.0

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1 Introduction

This document defines the reference models, mechanisms and procedures that are required to support network interworking between ATM and MPLS networks.

2 Scope

Comprehensive network interworking includes user data, signalling, routing, and management (including security) aspects. The scope of this specification is to specify the user plane interworking mechanisms and procedures between ATM and MPLS networks. It particularly specifies:

- List of requirements,
- Interworking scenarios,
- Interworking encapsulation format and semantics

for ATM-MPLS network interworking, where an intermediate MPLS network provides a transport service between two ATM networks.

This specification does not mandate or assume a particular link layer technology within the MPLS network.

3 References

The following references contain provisions that, through reference in this text, constitute provisions of this specification. At the time of publication, the editions indicated were valid. All references are subject to revision, and parties to agreements based on this specification are encouraged to investigate the possibility of applying the most recent editions of the references indicated below.

[1] IETF: RFC 3032 (January 2001): MPLS Label Stack Encoding

[2] ITU-T: Recommendation I.610 (02/99): B-ISDN operation and maintenance principles and functions

[3] ITU-T: Recommendation I.361 (02/99): B-ISDN ATM layer specification

[4] ITU-T: Recommendation I.732 (03/96): Functional characteristics of ATM equipment

[5] IETF: RFC 3031 (January 2001): Multiprotocol Label Switching Architecture

[6] ATM Forum: af-pnni-0055.000 (March 1996): Private Network-Network Interface Specification Version 1.0

[7] ATM Forum: af-sec-0100.002 (March 2001): ATM Security Specification Version 1.1

[8] ATM Forum: af-tm-0121.000 (March 1999): Traffic Management Specification Version 4.1

[9] ITU-T: Recommendation I.510 (March 1993): Definitions and General Principles for ISDN Interworking

4 Acronyms and terminology

4.1 Acronyms

AAL5	ATM Adaptation Layer Type 5
ATM	Asynchronous Transfer Mode
BOM	Beginning of Message
CDV	Cell Delay Variation
CLP	Cell Loss Priority
COM	Continuation of Message
CPCS	Common Part Convergence Sub-layer
CRC	Cyclic Redundancy Code
CTD	Cell Transfer Delay
EFCI	Explicit Forward Congestion Indication
EOM	End of Message
EXP	Experimental Bits
INE	Interworking Network Element
ISH	Interworking Specific Header
IWF	Interworking Function
LSP	Label Switched Path
LSR	Label Switching Router
MPLS	Multi-Protocol Label Switching
NMS	Network Management System
OAM	Operation Administration and Management
PCI	Protocol Control Information
PDU	Protocol Data Unit
PNNI	Private Network-Network Interface
PTI	Payload Type Identifier
RCC	Routing Control Channel
RM	Resource Management
S-bit	Stack bit
SSM	Single Segment Message
TTL	Time To Live
UU	User-to-User
VCC	Virtual Channel Connection
VCI	Virtual Channel Identifier
VPC	Virtual Path Connection
VPI	Virtual Path Identifier

4.2 Terminology

Interworking Function (IWF): The Interworking Function (IWF) is a functional entity that facilitates interworking between two dissimilar networks (e.g., ATM and MPLS). Additional details may be found in [9].

Interworking Network Element (INE): The INE provides user data plane, control plane and management plane interworking functions (IWF). The INE could be a standalone element, part of the ATM switch or part of an LSR.

Network interworking: In network interworking, the PCI (Protocol Control Information) of the protocol used in two similar networks and the payload information are transferred, transparently, across an intermediate network by a pair of IWFs.

Cell Concatenation: The process of bundling a group of cells belonging to a VCC or a VPC into a MPLS frame. Note that this is not AAL segmentation and reassembly.

5 Interworking Reference Models

This section specifies the reference models for two network interworking scenarios in which ATM-based networks and MPLS based networks are interconnected.

Figure 1 shows the reference model for ATM-MPLS-ATM interworking, where a MPLS network interconnects two ATM networks. INEs perform network interworking between the MPLS network and the ATM networks, enabling end-to-end ATM services between users on different ATM networks to be carried across the MPLS network.

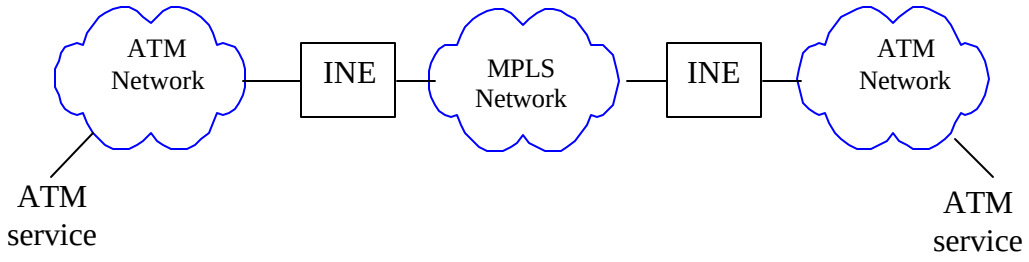


Figure 1: ATM-MPLS-ATM Interworking

Figure 2 shows the reference model for MPLS-ATM-MPLS interworking, where an ATM network interconnects two MPLS networks. INEs perform network interworking between the MPLS networks and the ATM network, enabling end-to-end services between users on different MPLS networks to be carried across the ATM network.

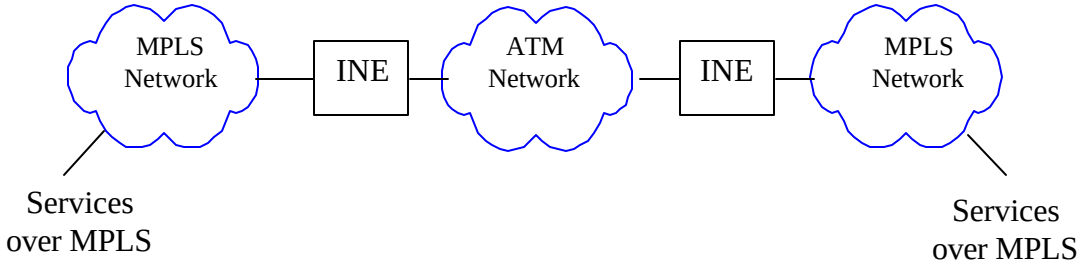


Figure 2: MPLS-ATM-MPLS Interworking

6 ATM-MPLS-ATM User Plane Interworking Aspects

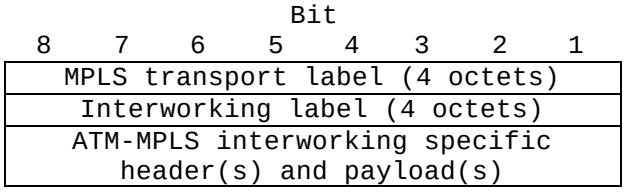
6.1 General Requirements

The general requirements for transparent transfer of ATM related information in the transfer (user) plane are:

- The ability to multiplex multiple ATM connections (i.e. VPCs and/or VCCs) into a MPLS LSP.
- Support for the traffic contracts and the QoS commitments made to the ATM connections.
- The ability to transparently carry all AAL types.
- The ability to transparently carry all OAM cells, including the support for proper operation of OAM PM cells and OAM security cells.
- Transport of Resource Management (RM) cells.
- Transport of Cell Loss priority (CLP) and Payload Type Indicator (PTI) information from the ATM cell header.
- The ability to encapsulate a single ATM cell within a single MPLS frame.
- The option to concatenate multiple cells into the same MPLS frame.
- The option to transport an AAL5 PDU into one or more MPLS frames for bandwidth efficiency.

6.2 Encapsulation Formats

Figure 3 shows the ATM-MPLS encapsulation format. It contains the MPLS Transport Label, the Interworking Label and ATM-MPLS Interworking Specific Header and the Payload.



Note: bit 8 is the most significant bit

Figure 3: ATM-MPLS Encapsulation Format

Figure 4 illustrates the relationship between the Transport Label and the Interworking Label.

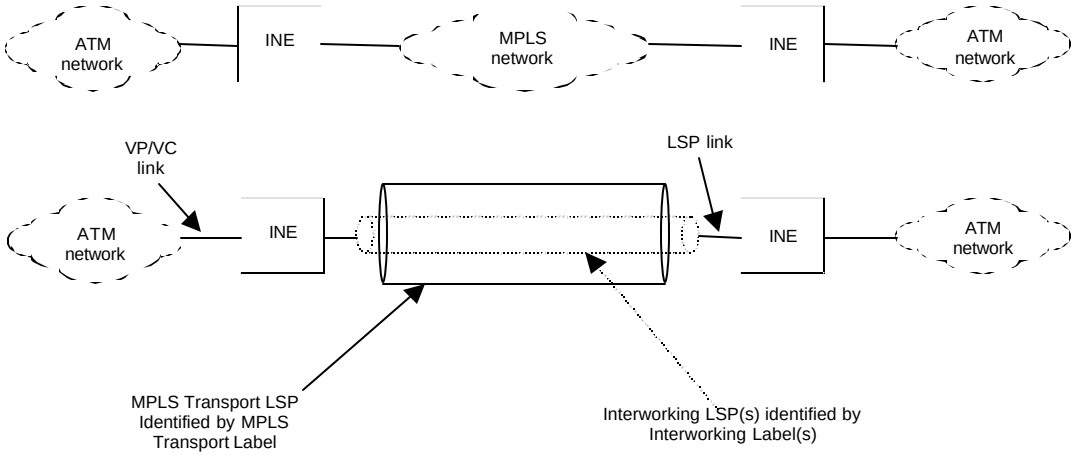


Figure 4: Relationship between MPLS transport label and the interworking label

6.2.1 MPLS transport label

This label identifies an LSP used to transport traffic between two ATM-MPLS interworking devices. This label is visible to the core LSRs, which use it to switch the transport LSP between core LSRs. The setting of the EXP and TTL fields of the transport label is outside the scope of this specification. The S bit is set to 0 for this label, indicating that this is not the bottom of the label stack.

6.2.2 Interworking label

The 4-octet interworking label uniquely identifies one interworking LSP, carried inside a MPLS transport LSP. The interworking label has the structure of a standard MPLS shim header (see Informative Appendix II). More than one interworking LSP may be supported by one Transport LSP.

Since a MPLS LSP is unidirectional, for the case of bi-directional ATM connections, there will be two different interworking LSPs, one for each direction of the connection. These may have different label values.

The IWF maintains context information that associates the ATM connection with the MPLS LSP. This information is referenced by means of the 20-bit label field of the interworking label.

The context of the interworking label field implies:

- Connection type: VCC or VPC.
- VPI value to be inserted in the ATM cells in the MPLS to ATM direction.
- For VCC connection types, the VCI value to be inserted in the ATM cells in the MPLS to ATM direction.

This does not preclude the inclusion of other context information.

Procedures for the generation and parsing of the interworking label are as follows:

ATM-to-MPLS direction
In the case of a VPC, translation of the VPI to the 20 bit label field is performed. In the case of a VCC, the VPI and VCI are translated to the 20-bit label field. This association is signaled or provisioned between a pair of peer IWFs.

The S bit is set to 1 to indicate the bottom of the label stack.

The settings of the EXP and TTL bits are for further study.

MPLS-to-ATM direction
In the case of a VPC, translation of the 20 bit label field to the VPI is performed. In the case of a VCC, the 20-bit label field is translated to the VPI and VCI. This association is signaled or provisioned between a pair of peer IWFs. MPLS frames received with an invalid or unassigned interworking label are discarded.

6.2.3 ATM-MPLS Interworking Specific Header (ISH)

This header is inserted before an ATM payload and identifies whether cells or frames are encapsulated in addition to other protocol control information. Note that length of the ISH depends on whether the VCI is present. Furthermore, the format of the ISH is different for cell and for frame encapsulation, and is specified in Section 6.3.

6.3 Encapsulation Modes

Three modes of encapsulation are defined for ATM-MPLS-ATM network interworking:

- Single cell encapsulation
- Concatenated cell encapsulation
- Frame encapsulation

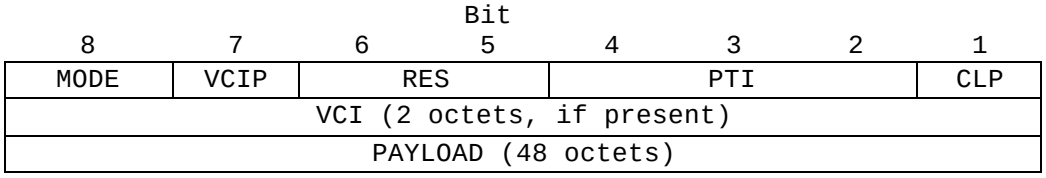
Support for single cell encapsulation is mandatory. All other encapsulations are optional.

6.3.1 Cell Mode Encapsulation (Single and Concatenated Mode)

One ATM cell or many concatenated ATM cells of an ATM VCC or VPC are encapsulated in a single MPLS frame. This specification mandates only the support of one ATM cell per MPLS frame, which is the default case. Support for encapsulation of multiple ATM cells per MPLS frame is optional. When ATM cells are concatenated, they

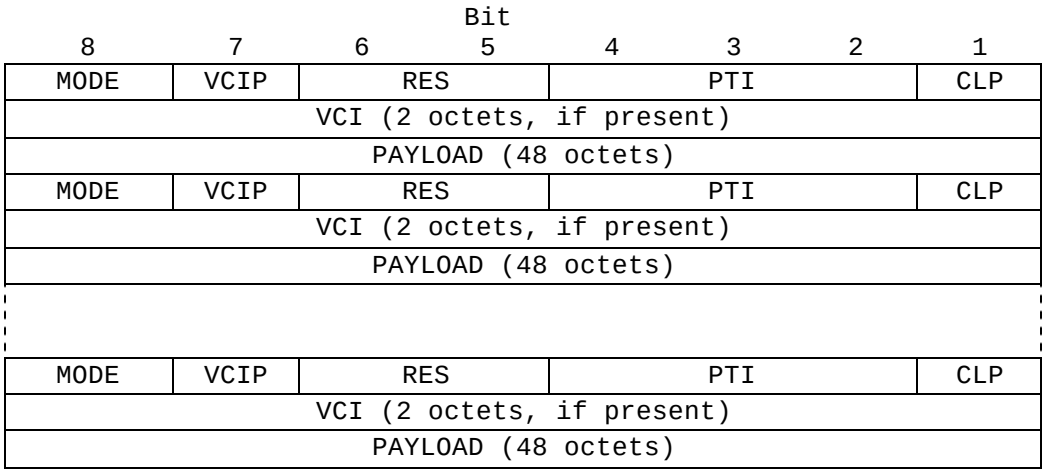
belong to the same ATM connection, VCC or VPC. In the case of a VPC, the concatenated cells may belong to different VCCs.

The encapsulation for cell mode, including the ATM-MPLS interworking specific header and payload, is shown in the following figures. Figure 5 shows the encapsulation for the single cell case, while Figure 6 shows the encapsulation for the concatenated cell case.



Note: bit 8 is the most significant bit

Figure 5: ISH and Payload for Cell Encapsulation of a Single Cell



Note: bit 8 is the most significant bit

Figure 6: ISHs and Payloads for Cell Encapsulation of Concatenated Cells

Description of the ATM-MPLS-ATM interworking specific header fields:

Bit #	**Field name**	**Field content explanation**
8	MODE	Identifies payload as a cell (= 0)
7	VCIP	VCI Present: set to “1” when the corresponding VCI field is present, set to “0” when no VCI field is present
6-5	RES	Reserved
4-2	PTI	This field is used to convey the PTI coding of each ATM cell
1	CLP	This field is used to convey the cell loss priority of each ATM cell
	VCI	This field, when present, is used to convey the VCI of an ATM cell

MODE (bit 8): This field is set to 0 to indicate cell mode.

VCIP (bit 7): For VCCs, the VCI field is not required and all instances of the VCIP field shall be set to 0.

Single cell encapsulation of VPCs: The VCI field is required and is transmitted with each cell. The VCIP field shall be set to 1.

Cell concatenation of VPCs: The VCIP field is set to 1 if the corresponding VCI field is present; otherwise the VCIP field is set to 0. If VCIP optimization is disabled (default), then the VCI field is present for every cell in the MPLS frame. If VCIP optimization is enabled, then the VCI field must be present in the following cases:

- The cell is the first cell within the MPLS frame
- The previous cell within the MPLS frame belongs to a different VCC

RES (bits 6-5): These bits are set to 0 and ignored upon reception.

PTI (bits 4-2): These bits are set to the value of the PTI field of the ATM cell header.

CLP (bit 1): This bit is set to the value of the CLP field of the ATM cell header.

VCI: This field, when present, is set to the value of the VCI field of the ATM cell header.

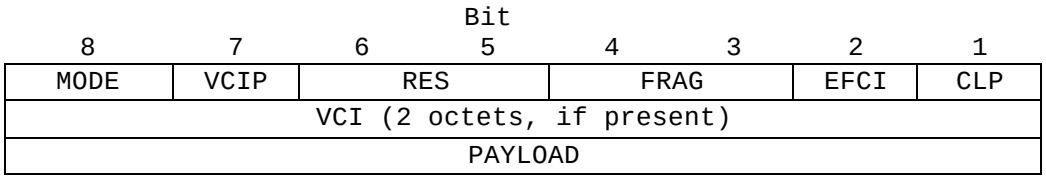
Payload: in the cell encapsulation mode, each payload field consists of the 48 byte payload of an ATM cell.

An objective of this encapsulation format is to avoid the unnecessary transmission of the VPI and VCI fields, when such information can be derived from the context information referenced by the interworking label.

6.3.2 Frame Mode Encapsulation

This mode is used for carrying AAL5 PDUs in the LSP tunnel. ATM cells of an AAL5 PDU are re-assembled and the resulting partial or complete AAL5 PDU is encapsulated in a MPLS frame.

In this mode, the whole AAL5 PDU (payload, padding, and whole AAL5 trailer, including UU, CPI, Length and CRC32) is encapsulated. The encapsulation for frame mode, including the ATM-MPLS-ATM interworking specific header and payload, is shown in Figure 7.



Note: bit 8 is the most significant bit

Figure 7: ISH and Payload for Frame Encapsulation

Description of ATM-MPLS interworking specific header fields:

Bit #	Field name	Field content explanation
8	MODE	Identifies payload as a frame (=1)
7	VCIP	VCI Present: set to "1" when the corresponding VCI field is present, set to "0" when no VCI field is present
6-5	RES	Reserved
4-3	FRAG	This field is used to support frame fragmentation. The following codepoints are defined: 0b00 = COM (Continuation of Message) 0b01 = EOM (End of Message) 0b10 = BOM (Beginning of Message) 0b11 = SSM (Single Segment Message)
2	EFCI	This field is used to convey the EFCI state of the ATM cells
1	CLP	This field is used to convey the cell loss priority of the ATM cells
	VCI	This field, when present, is used to convey the VCI of the ATM cells.

MODE (bit 8): This field is set to 1 to indicate frame mode.

VCIP (bit 7): In the case of a VPC, the VCIP field must always be set to 1, which means that the VCI field is present. In the case of a VCC, the VCIP field is set to 0, implying that the VCI field is not present.

RES (bits 6-5): These bits are set to 0 and ignored upon reception.

FRAG (bits 4-3): This field provides information about frame fragmentation. The fragmentation procedures are used to subdivide the AAL5 PDU into a series of fragments and later reassemble the sequence of such fragments to reconstitute the original AAL5 PDU.

EFCI (bit 2): This field is used to convey the EFCI state of the ATM cells. The EFCI state is indicated in the middle bit of each ATM cell's PTI field.

ATM-to-MPLS direction: The EFCI field of the ISH is set to the EFCI state of the last cell of the AAL5 PDU or AAL5 fragment.

MPLS-to-ATM direction: The EFCI state of all constituent cells of the AAL5 PDU or AAL5 fragment is set to the value of the EFCI field in the ISH.

CLP (bit 1): This field is used to convey the cell loss priority of the ATM cells.

ATM-to-MPLS direction: The CLP field of the ISH is set to 1 if any of the constituent cells of the AAL5 PDU or AAL5 fragment has its CLP bit set to 1; otherwise this field is set to 0.

MPLS-to-ATM direction: The CLP bit of all constituent cells for an AAL5 PDU or AAL5 fragment is set to the value of the CLP field in the ISH.

VCI: This field, when present, is set to the value of the VCI field of the constituent ATM cells.

PAYLOAD: The payload consists of the re-assembled AAL5 PDU (including the AAL5 padding and trailer) or the AAL5 PDU fragment.

An objective of this encapsulation format is to avoid the unnecessary transmission of the VPI and VCI fields, when such information can be derived from the context infomation referenced by the interworking label.

6.4 Configurable Parameters

For each ATM connection, the following parameters may be configured:

- Interworking labels (one for each direction)
- Connection type (VCC or VPC)
- Encapsulation mode
- MTU for the transport LSP
- Maximum number of concatenated cells in concatenated cell mode. This value is limited by the smallest link MTU in the transport LSP.
- VCIP optimization capability for VPCs in concatenated cell mode

Some of these parameters need to be agreed by the INEs at either end of the LSP.

6.5 Fragmentation

This section only applies only to frame mode encapsulation.

It may not always be possible to reassemble a full AAL5 frame at an INE. This may be due to the AAL5 PDU exceeding the MPLS MTU or if OAM cells arrive during reassembly of an AAL5 PDU. In these cases, the AAL5 PDU shall be fragmented. In addition, fragmentation may be desirable to bound ATM cell delay.

If no fragmentation occurs, then the FRAG bits are set to 11 (SSM, Single Segment Message).

When fragmentation occurs, the procedures described in the following subsections shall be followed.

6.5.1 Procedures in the ATM-to-MPLS direction

The following procedures shall apply while fragmenting AAL5 PDUs:

i. Fragmentation shall always occur at cell boundaries within the AAL5 PDU.

ii. For the first fragment, the FRAG bits shall be set to 10 (BOM, Beginning Of Message).

iii. For the last fragment, the FRAG bits shall be set to 01 (EOM, End Of Message).

iv. For all other fragments, the FRAG bits shall be set to 00 (COM, Continuation Of Message).

v. Setting of the EFCI and CLP fields in the ISH of the fragment shall be as per Section 6.3.2.

6.5.2 Procedures in the MPLS-to-ATM direction

The following procedures shall apply:

i. The 3-bit PTI field of each ATM cell header is constructed as follows:

   a) The most significant bit is set to 0, indicating a user data cell.
   b) The middle bit is set to the EFCI value of the ISH of the fragment.
   c) The least significant bit is set to 1 for the last ATM cell of a fragment where the FRAG bits are 01 (EOM) or 11 (SSM); otherwise this bit is set to 0.

ii. The CLP bit of each ATM cell header is set to the value of CLP field in the ISH.

6.6 ATM OAM and RM Cells

6.6.1 ATM-to-MPLS Direction

6.6.1.1 OAM Cells

Several types of OAM cells are defined in [2]. Applications, such as those identified in [7], utilize these OAM cells. These cells are categorized as:

- fault management cells
- performance monitoring and reporting, both in forward and backward directions
- user OAM cells (e.g. security OAM cells)

At the ATM layer, two types of OAM cell flows are identified: F4 (OAM flow on virtual path level) and F5 (OAM flow on virtual channel level). F4 and F5 OAM cells are either segment flows for communicating OAM related information within the boundary of the VPC or VCC, or end-to-end for information regarding end-to-end VPC or VCC operations. From an OAM perspective, the INE behaves as an ATM switch.

OAM cells are always encapsulated with the cell mode encapsulation, regardless of the encapsulation format for user data.

For cell mode encapsulation of user data, OAM cells are encapsulated in the same manner as user data cells.

For frame mode encapsulation of user data, OAM cells that arrive during the reassembly of an AAL5 frame cause fragmentation procedures to be invoked. The partially reassembled AAL5 frame is sent as a fragment, immediately followed by the OAM cell. Reassembly of the AAL5 frame is then resumed. If an OAM cell arrives between AAL5 frames, then it is sent in cell mode encapsulation. This procedure ensures cell sequence integrity for user cells and OAM cells.

The general functional architecture of an ATM network element is provided in Figure 4-2/I.732 of ITU-T Recommendation I.732 [4]. This functional model is used below to describe the treatment of F4 and F5 OAM cells at the INE.

The INE performs switching at either the VP or the VC level. In the following sections, “frame mode encapsulation” refers to the encapsulation method for user data.

VP Switching - Cell Mode Encapsulation
F4 OAM cells are processed by the INE according to the procedures specified in [2] and are then sent across the LSP. F5 OAM are not inserted or extracted here and are therefore simply encapsulated and sent across the LSP.

VP Switching - Frame Mode Encapsulation
This case is not supported by this specification.

VC Switching - Cell Mode Encapsulation
F4 OAM cells are inserted or extracted at the VP link termination; such OAM cells are not seen at the VC link termination and are therefore not sent across the LSP. F5 OAM cells are inserted or extracted at the VC link termination or VC termination according to the procedures specified in [2] and are then sent across the LSP.

VC Switching - Frame Mode Encapsulation
This case is the same as “VC switching – Cell Mode Encapsulation”.

6.6.1.2 RM cells

RM cells use a PTI value of 110 [2] and are treated the same way as OAM cells in order to maintain cell ordering.

6.6.2 MPLS-to-ATM Direction

OAM and RM cells are received as single encapsulated cells. They are treated at the INE in accordance with procedures described in [2], [4] and [7].

6.7 Interworking Transparency

6.7.1 General

An objective of this specification is to provide complete transparency for ATM services across the interworking function. Due to the nature of interworking across frame-based networks, several limitations are unavoidable.

The MPLS network is assumed to maintain frame sequence ordering between the sending IWF and the receiving IWF in steady state operation. Some applications are sensitive to the mis-ordering of user and OAM cells. (e.g. those described in [7]). Mechanisms for the detection of frames that are mis-ordered by the MPLS network are for further study.

The cell loss ratio may be adversely affected by transport across the MPLS network. An MPLS frame may be discarded due to a single bit error within the entire MPLS frame. By contrast, a separate HEC field protects ATM cell headers. Thus, ATM cells can be switched even if errors occur in the cell payload.

An INE has an implementation-specific contribution to the end-to-end maximum CTD and peak-to-peak CDV, when these parameters are specified for an ATM connection. The INE applies its contribution to the accumulated end-to-end values as specified in TM4.1 [8]. Once the connection is established, the INE's contribution to the maximum CTD and peak-to-peak CDV shall not exceed the values previously advertised. Note that the INE contribution includes the time required for cell concatenation (cell encapsulation mode) or AAL5 PDU reassembly (frame encapsulation mode).

At the time of publication, mechanisms for achieving QoS within an MPLS network were still evolving. Mappings of ATM service categories onto MPLS are for further study.

6.7.2 Frame Mode Encapsulation

This mode does not preserve the value of the CLP bit for every ATM cell within an AAL5 PDU. Therefore, transparency of the CLP setting may be violated. Additionally, tagging of some cells may occur when tagging is not allowed by the conformance definition [8].

This mode does not preserve the EFCI state for every ATM cell within an AAL5 PDU. Therefore, transparency of the EFCI state may be violated.

7 ATM-MPLS-ATM Control Plane Interworking Aspects

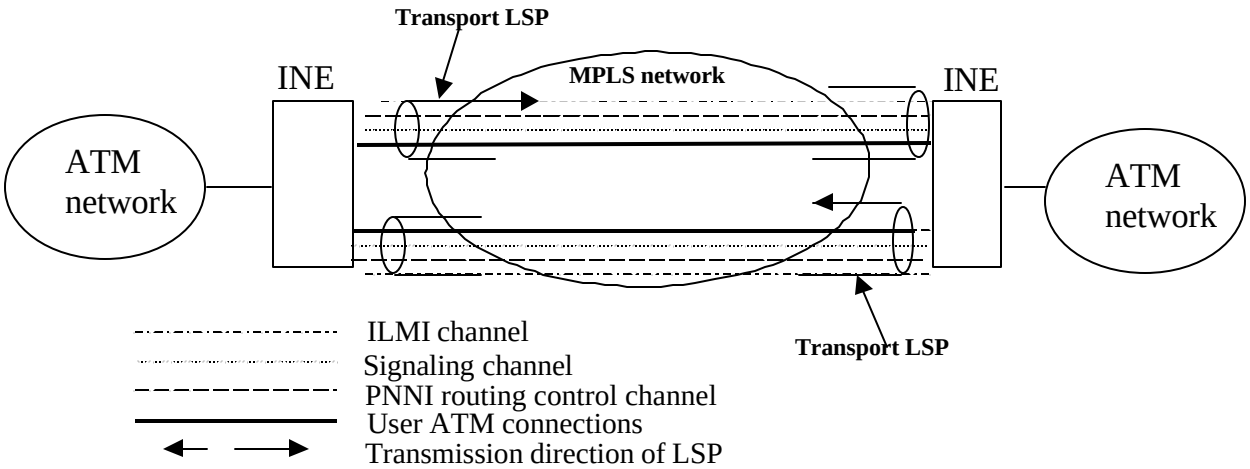


Figure 8: Connections to Support Control Plane

Transport of ILMI, control signaling and control routing requires configuration of the interworking labels to be used for each of these virtual connections.

From a PNNI perspective, MPLS transport LSPs are considered to be an abstraction of a PNNI physical link established between two PNNI nodes. For the ATM-MPLS-ATM network architecture, the role of PNNI routing protocols and ILMI is the same as in a traditional ATM PNNI network. The role of PNNI signaling is to establish MPLS interworking LSPs between INEs during ATM VCC or VPC establishment and to perform related signaling functions defined in the PNNI specification. These mechanisms are for further study.

Figure 8 shows various interworking LSPs (user ATM connections, signaling channel, routing control channel and ILMI channel) aggregated within the pair of transport LSPs.

The LSP labels of the 3 control channels are assigned and agreed upon by the two INEs.

Connection admission control (CAC) is one of the control plane functions that is used to achieve ATM QoS.

7.1 Signaling

In order to set up an ATM switched connection over the transport LSP, the INE negotiates the interworking label for each direction and then binds them to the corresponding VPI/VCI values on the ATM interfaces. Signaling mechanisms to accomplish this are for further study.

The establishment of transport LSPs is outside the scope of this specification.

7.2 Routing

The PNNI RCC is provisioned across the transport LSP. The transport LSP between the two INEs is seen as a single hop link by the PNNI routing protocol. Each INE is able to advertise link state changes, as specified in PNNI [6].

8 ATM-MPLS-ATM Management Plane Interworking Aspects

ATM OAM cells carry performance, fault, security and protection switching information for VCCs and VPCs on an end-to-end and segment basis [2] to support ATM layer management functions. The interworking function shall be capable of transferring ATM OAM information through the MPLS network by encapsulating ATM OAM cells in MPLS frames (see Section 6). In addition, the interworking function may correlate MPLS OAM information with ATM OAM information in the management plane through internal or external management interfaces. Correlation of MPLS OAM information and ATM OAM cells is for further study.

9 MPLS-ATM-MPLS User Plane Interworking Aspects

For further study

10 MPLS-ATM-MPLS Control Plane Interworking Aspects

For further study

10.1 Signaling

For further study

10.2 Routing

For further study

11 MPLS-ATM-MPLS Management Plane Interworking Aspects

For further study

Informative Appendix I: Example of ATM-MPLS-ATM Network Interworking

In this example (Figure 9), ATM is present at the network edge as the protocol that brings multiple services into the packet core (e.g. frame relay, voice services, and circuit emulation). ATM connections are carried transparently over MPLS LSPs from one edge of the packet core to another. The LSPs are primarily used as transparent tunnels. An ATM/MPLS interworking function at each edge of the core multiplexes a number of ATM connections (VCCs, VPCs or both) into a transport LSP and originates the transport LSP. The pair of transport LSPs (providing bi-directional connectivity) between any two interworking devices at the edge of the core is either established using a network management system or is initiated through MPLS signaling.

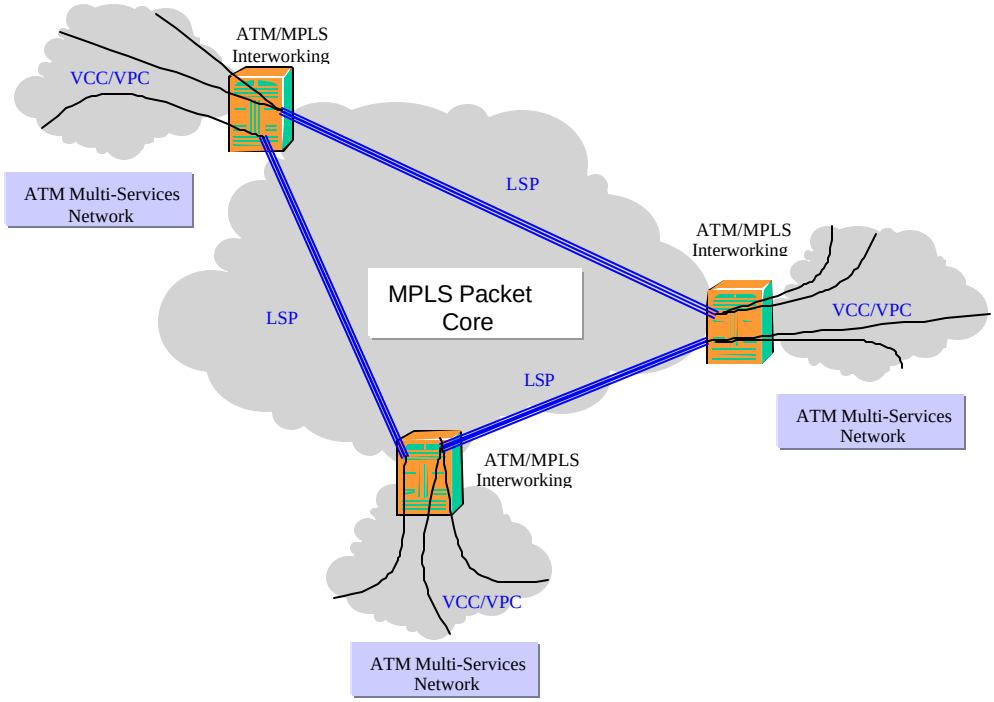


Figure 9: Example of ATM-MPLS-ATM Network Interworking

Transparency in this context means that ATM based services should be carried over the packet core unaffected. In this example, the interworking function is characterized by:

i. ATM and MPLS user data planes are interworked.

ii. ATM control plane information (signaling channels, routing control channels) and layer management plane information (OAM cells) are tunneled through the LSP from one ATM/MPLS edge to the other edge.

In this example, the recovery mechanisms of the ATM network are operational in the event a non-recoverable failure occurs in the MPLS core network. The following is an example of such a recovery operation. If a LSP fails in the MPLS network, the MPLS network is responsible for redirecting the traffic over a backup LSP. However, in some scenarios, the recovery may not be fast enough or may not be possible at all. In such cases, the MPLS network will have to generate a path failure indication back to the LSP originating points (i.e. the nodes where the interworking function resides). If the LSP between the 2 edges was originally signaled, it will be released back to its originating point via MPLS signaling procedures.

The LSP originating node, where the IWF resides, may act on the received failure indication to:

i. Generate the proper OAM cell type and content over the ATM PVCs towards the ATM network.

ii. Release ATM SVC calls back to their sources. ATM SPVC calls may be rerouted normally by their source nodes through an alternate path, which may or may not traverse the MPLS core. From the perspective of the

PNNI protocol, this operation is completely transparent and does not require any additional routing or signaling procedures.

Informative Appendix II: Structure of a MPLS Frame

A MPLS frame (packet) is made of a 4-octet header and the payload. The MPLS payload is made of the payload of the service, which it is carrying, plus other necessary information such as whole or part of the PCI (Protocol Control Information) of the payload. The encoding of the 4-octet MPLS frame header comprised of the label, EXP, S, and TTL fields, as specified in IETF RFC 3032 [1].

Informative Appendix III: Relationship Between ATM and LSP Connection Identifiers

Transport of ATM traffic over the MPLS network is performed using a two-level LSP stack. The outer label is the Transport LSP and provides the equivalent functionality of a transport link. The inner label is the Interworking LSP and provides support for VP/VC switching functions.

The transport LSP exists only within the MPLS network. It is used by the INE to provide a pseudo transmission path between interconnected INE devices. This provides the capability to perform ATM signaling and routing between INE devices.

Virtual Path Connections

When the INE is operating at the Virtual Path Connection (VPC) level, translation is performed between the ATM VPI and the IWF LSP label. This mode of operation is equivalent to performing virtual path switching in an ATM switch. The relationship between the ATM side of the INE and the MPLS side of the INE is shown in Figure 10.

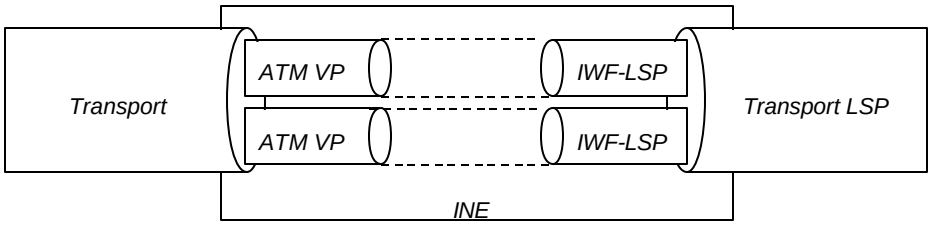


Figure 10: Relationship between VPC on ATM Side and LSP on MPLS Side of INE

An example of switching at the virtual path level is show in Figure 11.

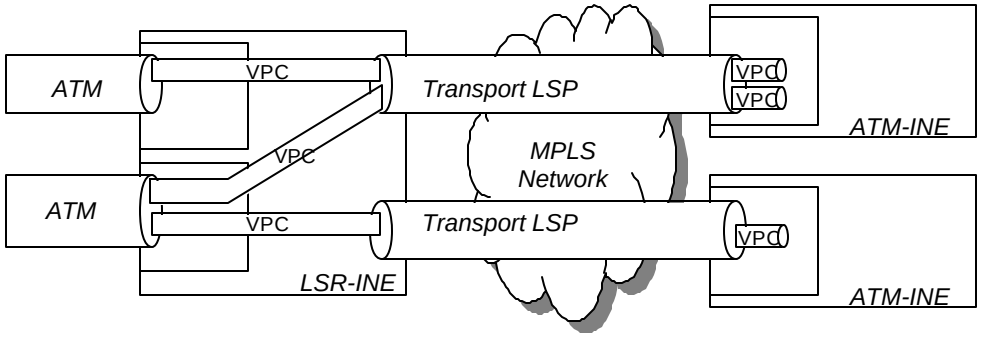


Figure 11: Switching at Virtual Path Level

Virtual Channel Connections

When the INE is operating at the Virtual Channel Connection (VCC) level, translation is performed between the ATM VPI/VCI and the IWF LSP label. This mode of operation is equivalent to performing virtual channels switching in an ATM switch. The relationship between the ATM side of the INE and the MPLS side of the INE is shown in Figure 12.

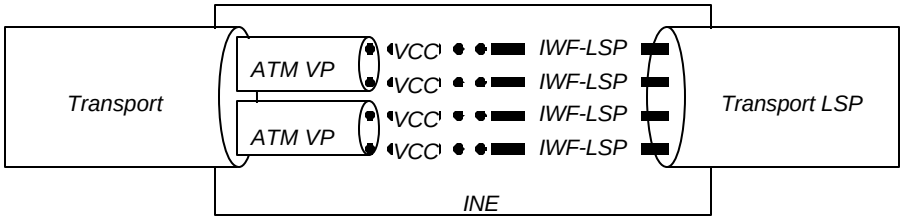


Figure 12: Relationship between VCC on ATM Side and LSP on MPLS Side of INE

An example of switching at the virtual channel level is show in Figure 13.

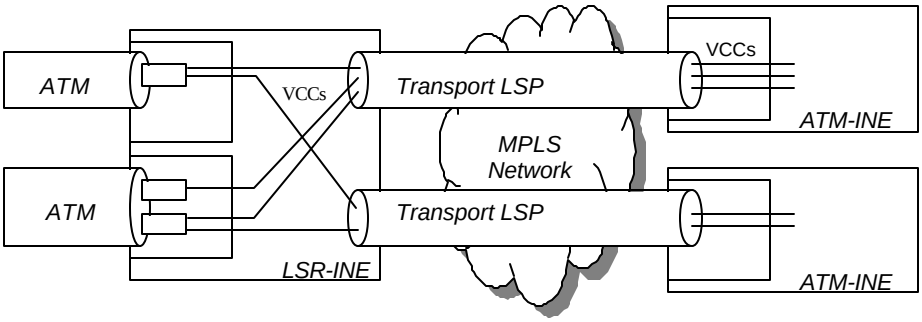
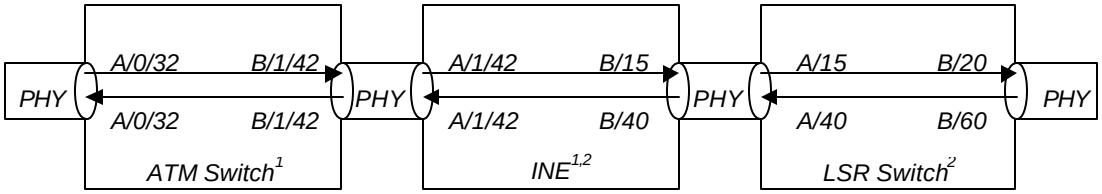


Figure 13: Switching at Virtual Channel Level

Relationship of ATM Connections and LSPs

An ATM connection is a bi-directional pair of virtual circuits that use the same identifiers for both directions of a communication channel. ATM switching can be viewed by examining only one of these directions. The ATM VP or VC arrives at the ingress side of an ATM switch. The input port/VPI/VCI is translated to the output port/VPI/VCI and switched based on the resulting values. Bi-directional communications is achieved by ensuring that switching of the output port/VPI/VCI maps back to the input port/VPI/VCI.

An LSP does not maintain this same relationship. The LSP label used in bi-directional communications is not required to have the same value. The relationship between an ATM switch, the INE and an LSP switch is shown in Figure 14.



Notes:
1. x/y/z refers to port/vpi/vci
2. p/q refers to port/label

Figure 14: Relationship between an ATM switch, the INE and an LSP switch

Providing a Transparent Transmission Path

The VPC connection mode of operation can be used to provide a transmission path capability. An INE operating in this mode presents a pseudo transmission service to the ATM connected devices. An ATM switch connected to the INE would appear to be directly connected to a corresponding ATM switch in the MPLS network

The Transport LSP is used to provide the pseudo transmission path. The INE algorithmically maps the ATM VPI to an LSP label e.g. by adding 16_{10} to the value of the VPI i.e. LSP = VPI + 16_{10}. Note that LSP values of 0-15 are reserved, and so the mapping operation must not cause wrapping to reserved label values.

The reverse operation is performed on the egress. The VCI is carried in the ISH. This usage of the Virtual Path mode is shown in Figure 15.

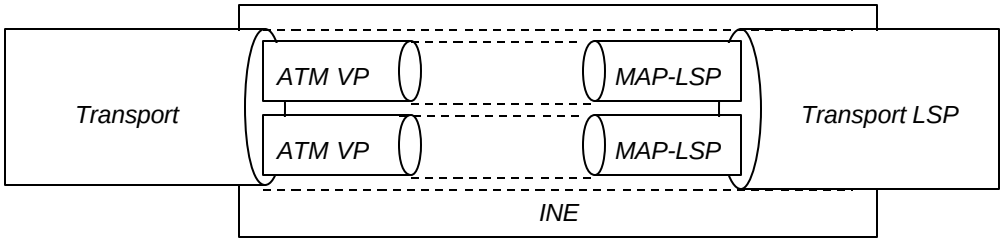


Figure 15: Usage of VPI Mapping to Provide Transparent Transport

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