The ATM Forum
Technical Committee

Cell-Based 1000 Mbit/s (CB1G) Physical Layer Specification over Single-mode or Multi-mode Fiber and Category 6 Twisted Pair Copper Cabling

af-phy-0162.000

April 2001

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Preface

This specification uses three levels for indicating the degree of compliance necessary for specific functions, procedures, or coding. They are indicated by the use of key words as follows:

- **Requirement**: "Shall" indicates a required function, procedure, or coding necessary for compliance. The word "shall" used in text indicates a conditional requirement when the operation described is dependent on whether or not an objective or option is chosen.
- **Objective**: "Should" indicates an objective which is not required for compliance, but which is considered desirable.
- **Option**: "May" indicates an optional operation without implying a desirability of one operation over another. That is, it identifies an operation that is allowed while still maintaining compliance.

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1 Introduction

Cell-Based Physical Layer specification provides the necessary functions to transport ATM cells directly on the physical media without using any frame structure. The functions of the full duplex physical layer (U-plane) are grouped into the Transmission Convergence (TC) sublayer (covered in section 2) and the Physical Media Dependent (PMD) sublayer (covered in section 3).

The Transmission Convergence sublayer is bit rate independent as it requires no frame structure. Due to the cell-based structure of the Transmission Convergence sublayer, transport capability of 997.685 Mbit/s is available at the ATM layer.

This specification also provides the OAM functions residing in the physical layer management (M-plane).

2 Transmission Convergence (TC) Sublayer

2.1 Physical layer cells

Physical Layer Cells include Physical Layer F3 OAM cells and idle cells. Physical Layer F3 OAM cells are used for operation and maintenance at the Transmission Path level. Idle cells are used for cell rate decoupling.

(R1) The first four octets of an idle cell header shall be as shown in Table 1. The cell payload content of an idle cell shall be "01101010" repeated 48 times. These values are given prior to scrambling.

Table 1 : Header pattern for idle cell identification

	Octet 1	Octet 2	Octet 3	Octet 4
Header Pattern	00000000	00000000	00000000	00000001

(R2) The first four octets of a Physical Layer F3 OAM cell shall be as shown in Table 2. The cell payload content of a Physical Layer F3 OAM cell shall be as indicated in subsection 2.4.3. These values are given prior to scrambling.

Table 2 : Header pattern for F3 OAM cell identification

	Octet 1	Octet 2	Octet 3	Octet 4
Header Pattern	00000000	00000000	00000000	00001001

2.2 Transmitter operation

2.2.1 Cell rate decoupling

(R3) The interface structure shall consist of a continuous stream of cells. Each cell contains 53 octets.

(R4) When there is no F3 OAM cell or ATM Layer cell to transmit, the physical layer shall insert idle cells for cell rate decoupling. Idle cells format is defined in subsection 2.1.

Note that the ATM layer can insert unassigned cells to perform cell rate decoupling. Unassigned cells are defined in ITU-T I.361 [3] and are part of the ATM layer cells. However, insertion of unassigned cells for cell rate decoupling is not required as this function is done at the physical layer by inserting idle cells.

2.2.2 Insertion of F3 OAM cells

(R5) One F3 OAM cell shall be inserted every 431 contiguous cells. F3 OAM cell insertion shall be done prior to any other cell.

The resulting cell stream consists in one F3 OAM cell followed by 431 contiguous cells (ATM layer cells or idle cells) and then another F3 OAM cell. The overhead induced by F3 OAM cell insertion is 1/432. The resulting interface transport capability is 997.685 Mbit/s.

2.2.3 Scrambling

Scrambling is used to improve the security and robustness of the HEC cell delineation mechanism as described in subsection 2.3.1. In addition it helps randomising the data in the information field for improvement of the transmission performance.

(R6) All the cells shall be scrambled by using the DSS (Distributed Sample Scrambler). The DSS shall scramble both the payload and the header (except the HEC field) of each cell.

The Distributed Sample Scrambler (DSS) is an additive Pseudo Random Binary Sequence (PRBS) scrambler that does not introduce error multiplication, and is of sufficiently high performance that an underlying PMD sublayer can rely on it to provide a high degree of randomisation. De-scrambling at the receiver is achieved by modulo addition of an identical locally generated pseudo random sequence having phase synchronisation with the first in respect of the transmitted cells. The scrambler does not affect the performance of the 8 bit HEC mechanism during Steady state operation.

Phase synchronisation of a receiver PRBS with polynomial generator order r is achieved by sending r linearly independent source PRBS samples through the transmission channel as conveyed data samples. When received without error these r samples are sufficient to synchronise the phase of the PRBS generator at the receiver to that of the transmitter PRBS generator.

A simple timing skew between the source PRBS samples and the conveyed PRBS samples serves as a means of decoupling the sample times of the source PRBS samples from the conveyed PRBS samples. This enables linear independence of PRBS samples to be simply achieved by taking samples at equal intervals of half an ATM cell (212 bits) from the source PRBS generator.

(R7) The transmitter pseudo random binary sequence shall be added (modulo 2) to the complete cell bit by bit excepting the HEC field. The pseudo random sequence polynomial shall be $x^{31}+x^{28}+1$.

(R8) The CRC octet for each cell shall then be modified by modulo 2 addition of the CRC calculated on the 32 bits of the scrambler sequence co-incident with the first 32 header bits. This is equivalent to calculation of the CRC on the first 32 bits of the scrambled header.

The first two bits of the HEC field are then modified as follows by two bits from the PRBS generator. The two bits from the PRBS generator will be referred to as the PRBS source bits and the two bits of the CRC onto which they are mapped will be referred to as the PRBS transport bits.

(R9) To the first HEC bit (HEC_8) it shall be added (modulo 2) the value of PRBS generator that was added (modulo 2) 211 bits earlier to the previous cell payload (U_{t-211}). To the second bit of the HEC field it shall be added (modulo 2) the current value of the PRBS generator (U_{t+1}). These samples are exactly half a cell apart (212 bits) and the first (U_{t-211}) is delayed by 211 bits before conveyance (requiring one D-type latch for storage) (211 bits is 1 bit less than half a cell).

Table 3 : PRBS phase (as added to payload and all header except HEC)

Ut-1	Ut	Ut+1	Ut+2	Ut+3	Ut+4	Ut+5	Ut+6	Ut+7	Ut+8	Ut+9

Table 4 : Resultant transmitted data element

CLP + Ut-1	HEC8 + Ut-211	HEC7 + Ut+1	HEC6	HEC5	HEC4	HEC3	HEC2	HEC1	1st pay_bit + Ut+8	2nd pay_bit + Ut+9

2.2.4 HEC generation

(R10) The HEC byte shall be generated as specified in Recommendation ITU-T I.432.1 [1] subsection 4.3.2.2. This shall include the recommended modulo 2 addition of the pattern "01010101" (55 hex) to the HEC bits.

2.2.5 Order of transmission of cells

(R11) Each cell shall be transmitted starting from the first byte of the cell header to the last byte of the cell payload (bytes are sent in increasing order).

2.3 Receiver operation

2.3.1 Cell delineation

Cell delineation is performed by using the correlation between the header bits to be protected (32 bits) and the relevant control bits (8 bits) introduced in the header by the HEC using a shortened cyclic code with generating polynomial $x^8 + x^2 + x + 1$. Figure 1 shows the state diagram of the HEC cell delineation method.

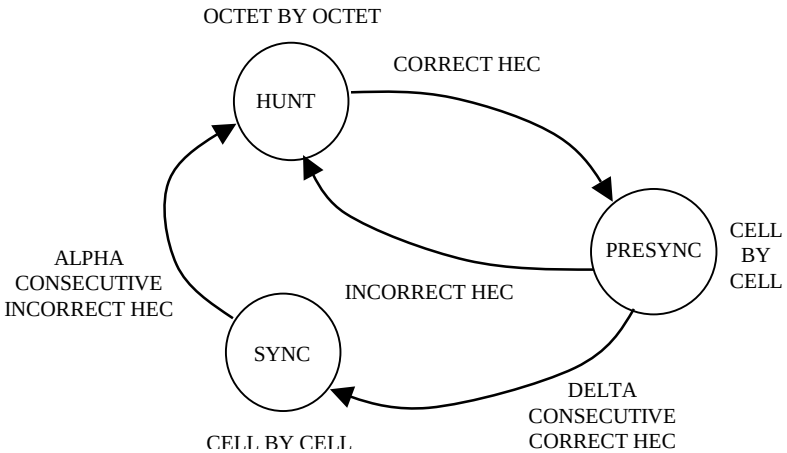

Figure 1 : Cell delineation state diagram

(R12) In the HUNT state, the delineation process is performed by checking octet by octet for the correct HEC (i.e. syndrome equals zero) for the assumed header field. Prior to scrambler synchronisation, only the last six bits of the HEC are to be used for cell delineation checking. Once such an agreement is found, it is assumed that one header has been found, and the process enters the PRESYNC state.

(R13) In the PRESYNC state, the delineation process is performed by checking cell by cell for the correct HEC. Prior to scrambler synchronisation, only the last six bits of the HEC are to be used for cell delineation checking. The process repeats until the correct HEC has been confirmed DELTA times consecutively, at

which point the process moves to the SYNC state. If an incorrect HEC is found, the process returns to the HUNT state. The total number of consecutive correct HEC required to move from the HUNT state to the SYNC state is therefore DELTA + 1.

(R14) In the SYNC state the cell delineation will be assumed to be lost if an incorrect HEC is obtained ALPHA times consecutively.

(R15) Cells with correct HEC shall be passed to the ATM layer when the cell delineation process is in SYNC state and the descrambler is in Steady state operation. In any case, idle cells and Physical Layer OAM cells shall not be passed to the ATM layer.

(R16) The value of ALPHA shall be equal to 7. The value of DELTA shall be equal to 8.

2.3.2 HEC verification

(R17) HEC sequence error detection shall be performed as specified in Recommendation ITU-T I.432.1 [1] subsection 4.3.2.1. This shall include only error detection as single bit error correction is not applicable due to the error multiplication introduced by the 8B10B coding performed in the PMD sublayer.

2.3.3 Descrambling

Three basic states of descrambler operation are defined :

(I) Acquisition of scrambler synchronisation
(II) Verification of descrambler synchronisation
(III) Steady state operation

The transition between these three states is based on the value of a confidence counter (C).

Receiver state (I): Acquisition of scrambler synchronisation

(R18) The descrambler shall enter this state at start-up and each time the cell delineation process enters the HUNT state. When entering this state the confidence counter shall be reset to 0 (C=0).

Cell delineation:

The cell delineation mechanism is independent of the descrambler synchronisation mechanism. However while the descrambler is in Acquisition or Verification states, the cell delineation is determined by using only the last six bits of the HEC field. This is because the first two bits of the HEC field have been modified by the modulo 2 addition of the conveyed data samples and cannot therefore be used in delineation or HEC evaluation until the descrambler is synchronised (Steady state operation).

Acquisition of scrambler synchronisation:

(R19) In Acquisition state, the conveyed samples (U_{t-211},U_{t+1}) shall be extracted from the bit stream by modulo 2 addition of the predicted values for HEC_8 and HEC_7 to the received values. The predicted values correspond to bits HEC_8 and HEC_7 of the HEC value calculated over the first four bytes of the received header.

(R20) The conveyed bits (U_{t-211},U_{t+1}) shall be used as samples for descrambler synchronisation in the receiver. As the degree of the scrambler polynomial is equal to 31, the number of consecutive error free conveyed samples needed to synchronise the descrambler is equal to 31 (16 cells).

Descrambler synchronisation may be achieved by comparing, every 212 bits, the received sample bit to the corresponding bit locally generated by the descrambler (Figure I-1). If these two bits are not identical a constant correction vector is applied to the descrambler through feedforward taps. At time t, the sample conveyed in HEC_8 (U_{t-211}) is compared to the descrambler bit V_{t-211} generated at time t-211. At time t+212, the sample conveyed in HEC_7 (U_{t+1}) is compared to the descrambler bit V_{t+1} generated at time t+1 (both U_{t+1} and V_{t+1} have been stored during 211 bits before being compared). Because both conveyed samples are compared to the corresponding descrambler bits 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feedforward taps are chosen to generate a sequence that is advanced by 211 samples (Figure I-1).

(R21) For every cell received correctly with no errors detected in HEC bits 1 to 6 the confidence counter shall increment (C=C+1). Any error detected in HEC bits 1 to 6 results in a return to the initial state (C=0). When the confidence counter reaches the value of 16 the descrambler process shall enter the Verification state.

Time to achieve scrambler synchronisation:

Two bit samples are conveyed per cell, which are linearly independent. The number of consecutive error free conveyed samples needed to synchronise the descrambler is equal to the degree of the scrambler polynomial, therefore 16 cells provide the 31 samples necessary to synchronise the descrambler.

The descrambler synchronisation process is not disabled during cell delineation, however the descrambler will not begin to converge until the cell delineation mechanism has located the true position of the HEC field in the header and is no longer in its HUNT state. Therefore the start of descrambler synchronisation acquisition convergence will be coincident with the final transition from the HUNT state to the PRESYNC state of the cell delineation mechanism.

Receiver state (II): Verification of descrambler synchronisation

The Verification state differs from the Acquisition state in that the recursive descrambler is assumed to be synchronised and is no longer modified with synchronising samples. Verification is needed because errors undetectable by the 6 bits HEC check may have occurred in the conveyed bits during the Acquisition state (resulting in incorrect descrambler synchronisation). The verification phase tests the predicted PRBS generated locally by the descrambler against the remote reference sequence given by the conveyed samples. To verify descrambler Acquisition phase overall such that the probability of false descrambler synchronisation is less than 10^{-6} requires 16 verifications (8 cells) where the transmission ratio is better than 10^{-3}.

(R22) In Verification state, the conveyed samples (U_{t-211},U_{t+1}) shall be extracted from the bit stream by modulo 2 addition of the predicted values for HEC_8 and HEC_7 to the received values. The predicted values correspond to bits HEC_8 and HEC_7 of the HEC value calculated over the first four bytes of the received header.

(R23) For each cell received without detected errors in HEC bits 1 to 6, the conveyed samples (U_{t-211},U_{t+1}) shall be compared to the corresponding PRBS bits generated locally by the descrambler (V_{t-211},V_{t+1}). For each cell with two correct predictions received, the confidence counter shall increment (C=C+1). If one or two incorrect predictions are made then the confidence counter shall decrement (C=C-1).

(R24) If the confidence counter falls below the value of 8, the descrambler process shall return to the Acquisition state and the confidence counter is reset (C=0).

(R25) When the confidence counter reaches the value of 24, the descrambler process shall enter the Steady state operation.

Receiver state (III): Steady state operation (synchronised scrambler)

In this state the HEC_8 and HEC_7 bits can both be returned to normal use following their descrambling by using the bits generated locally (V_{t-211},V_{t+1}). Properties of error detection and correction are not affected by this process. Both cell delineation and descrambler synchronisation robustness to channel bit-slip are reliably monitored in this state by the existing cell delineation state machine.

(R26) In this state, the two PRBS bits generated locally by the descrambler shall be used to extract the two conveyed samples (U_{t-211},U_{t+1}) by modulo addition. Therefore bits HEC_8 and HEC_7 can both be returned to normal use. Properties of error detection and correction are not affected by this process.

(R27) When the cell delineation process detects a non-zero syndrome with error bits confined to bits HEC_8 and HEC_7 the confidence counter shall decrement (C=C-1), else it shall increment (C=C+1). The confidence counter shall have an upper limit of 24.

(R28) If the confidence counter falls below the value of 16 or if the cell delineation process returns to the HUNT state, the descrambler process shall return to the Acquisition state.

2.3.4 Extraction of physical layer cells

(R29) Idle cells shall be extracted, as these cells shall not be passed to the ATM layer.

(R30) Physical Layer F3 OAM cells shall be extracted for maintenance and performance monitoring functions. These cells shall not be passed to the ATM layer.

2.4 OAM functionality

2.4.1 Maintenance signals

(R31) Transmission Path Remote Defect Indication (TP-RDI) shall be provided to alert the upstream equipment in the opposite direction of transmission that a defect has been detected along the downstream path. It shall be set when a Loss Of Cell Delineation (LCD), Loss of Maintenance flow (LOM), or Loss of Signal (LOS) has been detected at the path level. The time to set this signal must be as short as possible but long enough to filter intermittent defect information. The coding of this field is defined in subsection 2.4.3.

Description of defects:

Loss of Signal (LOS) - LOS is considered to have occurred when the amplitude of the relevant signal has dropped below prescribed limits for a prescribed period.

Out of Cell Delineation (OCD) - An OCD anomaly occurs when the cell delineation process changes from SYNC state to HUNT state while in a working state (refer to Figure 1). An OCD anomaly terminates when the PRESYNC to SYNC state transition occurs (refer to Figure 1) or when the OCD anomaly persists and the LCD maintenance state is entered (see below).

Loss of Cell Delineation (LCD) - An LCD defect occurs when an OCD anomaly (see above) has persisted for x ms. An LCD defect terminates when the cell delineation process (refer to Figure 1) enters the SYNC state. The value of x shall be in the range 1 to 4.

Loss of Maintenance (LOM) - Loss of one F3 OAM cell is detected when no F3 OAM cell is received 431 cells after the last received F3 OAM cell. LOM defect is declared when two successive anomalies (loss of one F3 OAM cell) are detected.

2.4.2 Transmission performance monitoring

Transmission performance monitoring is performed to detect and report transmission errors. At the Transmission Path level, this function is achieved by using Physical Layer F3 OAM cells.

Physical Layer F3 OAM cells are inserted on a recurrent basis (every 431 cells) in the cell flow. Each F3 OAM cell monitors 8 logic blocks of 54 cells each. For each monitored block, performance monitoring is achieved by checking the BIP-8 value. The BIP-8 calculation is performed only on the cell payload because the cell header is already monitored by the HEC field.

Upon reception of one F3 OAM cell, the receiver determines the number of BIP-8 violation in each monitored block. The performance is then calculated according to anomalies a1 to a4 defined in Recommendation ITU-T G.826 Annex D [4]. The total number of error blocks detected in one direction between two consecutive F3 OAM cells is sent in the opposite direction of transmission by using the REB field (subsection 2.4.3). Therefore both the transmitter and the receiver have the same view of the performance measured in one particular direction of transmission.

2.4.3 Allocation of OAM functions in information field

(R32) F3 OAM cell payload shall be allocated as defined in Table 5.

Table 5 : Allocation of OAM functions in information field

1	R	25	R
2	R	26	R
3	PSN	27	R
4	R	28	R
5	R	29	R
6	R	30	RDI
7	R	31	R
8	EDC-B1	32	R
9	EDC-B2	33	R
10	EDC-B3	34	R
11	EDC-B4	35	R
12	EDC-B5	36	R
13	EDC-B6	37	R
14	EDC-B7	38	R
15	EDC-B8	39	R
16	R	40	R
17	R	41	R
18	R	42	R
19	R	43	R
20	R	44	R
21	R	45	R
22	R	46	REB
23	R	47	CEC (2) Note 1
24	R	48	CEC (8) Note 1

Note 1: MSB is bit 2 of byte 47 and LSB is bit 1 of byte 48.
Bits 3 to 8 of byte 47 are set to 0.

(R33) PL-OAM Sequence Number (PSN): this field shall be used to number the F3 OAM cells. It is designed to have a sufficiently large cycle compared with the duration of cell loss and insertion. 8 bits are allocated to PSN. The counting is then done modulo 256. This field shall be incremented by one at each new F3 OAM cell being sent.

(R34) Error detection code (EDC): this code shall be a BIP-8 calculated on a block of 54 cells repeated for each monitored block. The number of monitored blocks is equal to 8. The field EDC-Bn shall correspond to the BIP-8 calculated on the monitored block number n. For F3 OAM cell number n, the first monitored block

shall begin with the first cell following the F3 OAM cell number n-1. The last monitored block shall end at the end of the F3 OAM cell number n, as indicated in Figure 2.

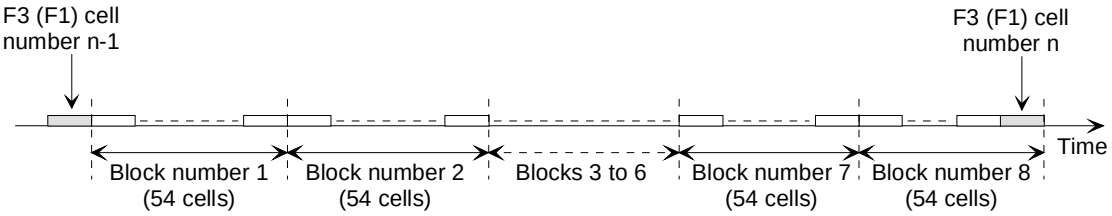

Figure 2 : Definition of the monitored block boundaries

F3 OAM cells shall not be taken into account by the BIP-8 calculation. This means the BIP-8 calculation shall be stopped during F3 OAM cells. For the other cells (ATM layer cells and idle cells) the BIP-8 shall be calculated only on the cell payload before the scrambling is performed.

One octet is allocated for each EDC-Bn field. Each bit of the EDC-Bn field shall be equal to the BIP calculated on the same range bits of each monitored octet (i.e. the Most Significant Bit of each EDC-Bn octet shall be equal to the BIP calculated on the Most Significant Bit of each octet of the monitored block).

(R35) Remote Error Blocks (REB): This field shall indicate to the far end direction the total number of error blocks between two consecutive F3 OAM cells in accordance with anomalies a1 to a4 defined in Annex D of ITU-T Recommendation G.826 [4]. The REB field shall be the value of a running counter (modulo 256) increased periodically by the number of error blocks detected in one direction of transmission (in accordance with G.826 Annex D). The value of this running counter shall be put in the REB field of each F3 OAM cell being sent in the opposite direction. By subtracting the values contained in the REB fields of two consecutively received valid F3 OAM cells (i.e. CEC field indicates a valid cell payload), the receiving system knows the total number of error blocks measured by the far end system.

(R36) Transmission Path Remote Defect Indication (TP-RDI): This field shall be used to alert the upstream equipment in the opposite direction of transmission that a defect has been detected along the downstream path. The possible defects are LOM, LCD, and LOS. The coding of this field shall be as indicated in Table 6.

Table 6 : Coding of TP-RDI defect information

MSB							LSB
0	0	0	0	LOM	LCD	LOS	RDI_indication

When a defect is detected (LOM, LCD, or LOS), the corresponding bit shall be set to 1, else it shall remain 0. When at least one defect is detected, the RDI_indication bit shall be set to 1, else it shall remain 0.

(R37) Cell Error Control (CEC) is used to detect errors in the cell payload. A CRC 10 shall be used (it should be the same as in the F4/F5 flows). When the CEC value indicates an invalid payload the F3 OAM cell is considered in error and an anomaly is raised (refer to Recommendation ITU-T G.826 [4]). Similarly when the HEC value indicates an invalid header the F3 OAM cell is also considered in error and an anomaly is raised (refer to [4]).

(R38) Reserved Field (R) shall contain the octet pattern of " 01101010 " (6A hex), which is the same as that of the idle cells.

3. Physical Medium Dependent (PMD) Sublayer

Physical layer cells are transferred between the Transmission Convergence (TC) sublayer (described in section 2) and the ATM Physical Median Dependent (PMD) sublayer covered in this section. The ATM full duplex PMD sublayer is divided into a coding sublayer, which is media independent, and a media dependent Ten Bit Interface PMD (TBI PMD) sublayer. The currently supported TBI PMD's are specified in subsection 3.5. Link synchronization and loss of synchronization are also specified in the coding sublayer.

3.1 Coding sublayer

(R39) Physical layer cells transferred between the coding sublayer and the TBI PMD sublayer shall be encoded (or decoded) eight bits at a time into 10-bit data characters.

In addition some of the remaining 10-bit characters are used to represent special characters for control, Kx.y, defined in Table 8. The coding sublayer will use two of the special characters for synchronization and the start of data transmission. Other uses for the characters can be found in 802.3 IEEE Standard, 2000 edition [8] and TR/X3.18-1997 ANSI Technical Report [9].

3.1.1 Data characters

Encoding or decoding of valid 10-bit data or special characters will use a running disparity (RD) calculation to determine the correct character from two possible choices. The two choices given in Tables 7 and 8, correspond to the current value of the running disparity. Running disparity is a binary value with either a negative value (-) or positive value (+).

(R40) The coding sublayer shall maintain a running disparity calculation to generate the correct transmitted and received 10-bit data or special characters. Subsection 3.1.5 specifies the rules for running disparity calculation. Additional information may be found in 802.3 IEEE Standard, 2000 edition [8] and TR/X3.18-1997 ANSI Technical Report [9]. Decoding violations during data reception, a received 10-bit data character with an incorrect disparity, shall be passed on as decoded to the TC sublayer. A decoded character that is not defined in Table 7 received during normal data reception by the PMD shall be passed on to the TC sublayer as hex FF.

3.1.2 Special characters

(R41) A special character followed by a data character shall define a code group, K28.5/D5.6 and K28.5/D16.2, used for link synchronization. The special character K28.5 shall always be transmitted on even boundaries (characters 0, 2, 4, etc.) in the character stream. The coding sublayer shall continuously transmit data or special characters to the TBI PMD. The start of data transmission shall be indicated by the transmission or reception of the K27.7 special character.

Auto-negotiation or use of other special characters for configuration and control is not specified and beyond the scope of this specification. Decoded characters during synchronization should not be transmitted to the TC sublayer.

3.1.3 Comma

In a 10-bit character the seven bit string "0011111" is defined as a comma+ and "1100000" as a comma-. The comma in K28.5 is a singular bit pattern and cannot appear in any other location of a code group in the absence of errors and cannot be generated across the boundaries of any two adjacent code groups used in this specification. See 802.3 IEEE Standard, 2000 edition [8] and TR/X3.18-1997 ANSI Technical Report [9] for other circumstances. The comma is used to obtain character and code group alignment.

3.1.4 10-bit character

(R42) Table 7 specifies the coding of the eight bits of data and 10-bit data characters for the current negative or positive running disparity, RD- and RD+. Table 8 specifies the coding of the 10-bit special characters. Only K28.5 and K27.7 are used in this specification.

Table 7 : 10-bit data characters

D[0:31, 0:7]	Data Eight Bit Value	Current RD- abcdei fghj	Current RD+ abcdei fghj	D[0:31, 0:7]	Data Eight Bit Value	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	100101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001001 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00101	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00111	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 01001	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 01011	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 01100	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01111	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 10001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011

D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001

D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 8 : 10-bit special characters

Kx.y Special Character	Current RD-	Current RD+
	abcdei fghj	abcdei fghj
K28.0	001111 0100	110000 1011
K28.1	001111 1001	110000 0110
K28.2	001111 0101	110000 1010
K28.3	001111 0011	110000 1100
K28.4	001111 0010	110000 1101
K28.5	001111 1010	110000 0101
K28.6	001111 0110	110000 1001
K28.7	001111 1000	110000 0111
K23.7	111010 1000	000101 0111
K27.7	110110 1000	001001 0111
K29.7	101110 1000	010001 0111
K30.7	011110 1000	100001 0111

3.1.5 Disparity calculation

(R43) Running disparity of a character shall be calculated on the two sub-blocks, abcdei then fghj. Running disparity at the end of a sub-block is positive if the sub-block contains more ones than zeros or if abcdei is 000111 or fghj is 0011. Running disparity shall be negative if the sub-block contains more zeros than ones or if abcdei is 111000 or fghj is 1100. Otherwise running disparity shall be the same as at the beginning of the sub-block. The running disparity at the end of a character shall be the current running disparity used for the next character.

3.2 Ten bit interface (TBI)

The interface between the TC sublayer and coding sublayer is not intended as a separate physical interface or accessible. It is expected that the TBI may be implemented as a chip to chip interface from the coding sublayer to a TBI PMD. This would allow support for the different TBI PMD's defined in subsection 3.5.

3.2.1 Signals

The interface signals for the TBI PMD are defined in Table 9.

Table 9 : Signal definitions

Symbol	Signal Name	Signal Type	Active Level
TX[0:9]	Transmit Data	Input	H
TBC	Transmit Byte Clock	Input	↑
EWRAP	Enable Wrap	Input	H
RX[0:9]	Receive Data	Output	H
RBC[0]	Receive Clock 0	Output	↑
RBC[1]	Receive Clock 1	Output	↑
COM_DET	Comma Detect	Output	H
LCK_REF	Lock to Reference	Input	L
REFCLK	Reference Clock	Input	↑
EN_CDET	Enable Comma Detect	Input	H

TX[0:9] is the 10-bit parallel data interface to the TBI PMD. The bit TX[0] corresponds to "a" in the 10-bit encoded character and is transmitted first in a serial transmission TBI PMD.

TBC is the 125 MHz transmit clock to the TBI PMD. This clock is used to latch the TX[0:9] into the TBI PMD. The TBC is frequency locked to any REFCLK.

EWRAP is used to wrap the TBI PMD transmit characters back to the input. Use of this function is not defined in this standard.

RX[0:9] is the 10-bit parallel data interface from the TBI PMD. The bit RX[0] corresponds to "a" in the 10-bit encoded character and is received first in a serial transmission TBI PMD.

RBC[0] is the 62.5 MHz receive clock from the TBI PMD and is used to receive odd characters (1, 3, etc.). This clock may be stretched during comma alignment.

RBC[1] is the 62.5 MHz receive clock from the TBI PMD and is used to receive even characters (0, 2, etc.). RBC[1] is 180° out of phase with RBC[0]. This clock may be stretched during comma alignment.

COM_DET indicates that the data character associated with the current RBC[1] contains a valid comma.

LCK_REF causes the TBI PMD to lock its PLL to REFCLK. Use of this function is not defined in this standard but may be helpful in acquiring initial lock to the incoming bit stream.

(R44) REFCLK is a 125 MHz transmit reference clock. The frequency tolerance for this clock shall be +/- 100ppm.

EN_CDET enables the TBI PMD to align the 10-bit field on a comma. The TBI PMD may delete one or more characters and stretch the receive clock in order to align the received comma with RBC[1].

3.2.2 Electrical characteristics

Table 10 defines the electrical characteristics for the TBI PMD.

Table 10 : Electrical characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VOH	Output High Voltage	IOH = -400uA	VCC = Min	2.2	3.0	VCC	V
VOL	Output Low Voltage	IOL = 1 mA	VCC = Min	GND	0.25	0.6	V
VIH	Input High Voltage			2.0	-	VCC+10%	V
VIL	Input Low Voltage			GND	-	0.8	V
IIH	Input High Current	VCC = Max	VIN = 2.4 V	-	-	40	uA
IIL	Input Low Current	VCC = Max	VIN = 0.4 V	-	-	-600	uA
Cin	Input Capacitance			-	-	4.0	pf
tr	Clock Rise Time	0.8V to 2.0V		0.7	-	2.4	ns
tf	Clock Fall Time	2.0V to 0.8V		0.7	-	2.4	ns
tr	Data Rise Time	0.8V to 2.0V		0.7	-	-	ns
tf	Data Fall Time	2.0V to 0.8V		0.7	-	-	ns

3.3 Synchronization

The PMD sublayer is divided into a local encoding-transmit and receive-decoding operation; representing a full duplex channel. These are synchronized with the equivalent remote upstream equipment on the channel. At the start of synchronization the received bit stream is aligned on a comma in the K28.5 character and a code group, K28.5/D5.6 (or K28.5/D16.2). Once the code group is aligned the code group K28.5/D16.2 is transmitted to notify the remote equipment. Receipt of this code group is used to indicate that physical layer cells can now be transmitted. The special character K27.7 is used to indicate the start of data character transmission. Synchronization for the receiver and transmitter follow two different state diagrams.

The receiver starts synchronization at power up, when a local Loss of Signal (LOS) =1 is indicated by the TC sublayer, a remote LOS = 1 is received by the Transmission Path Remote Defect Indication (TP-RDI), or when a local Loss of Cell Delineation (LCD) = 1 and is transmitted to the remote equipment by the TP-RDI. Once the receiver is aligned on a comma then the local LOS is set to 0. Figure 3 illustrates the receiver synchronization.

The transmitter starts synchronization at power up, a local LOS = 1, a remote LOS = 1, or remote LCD = 1 is received. If the LOS = 0 and the remote status OK is true the transmitter would send a block of 47 octets and then return to normal transmission. Figure 4 illustrates the transmitter synchronization.

(R45) At power up, a local LOS = 1, a remote LOS = 1 is received, or local LCD = 1 and is transmitted to the remote equipment by the TP-RDI; the receiver shall set the remote status OK to not true and align the received bit stream on a comma to the leftmost bit positions of an even character (EN_CDET).

(R46) When the receiver has detected three successive commas in the leftmost bit positions of an even character (COM_DET), the LOS shall be set to a 0, and the receiver shall assume an initial negative running disparity and begin decoding code groups.

(R47) On the receipt of a K28.5/D16.2 code group by the receiver with the correct disparity, the receiver shall set the remote status OK to true.

(R48) On the receipt of a K27.7 special character by the receiver, the receiver shall begin the reception of data characters.

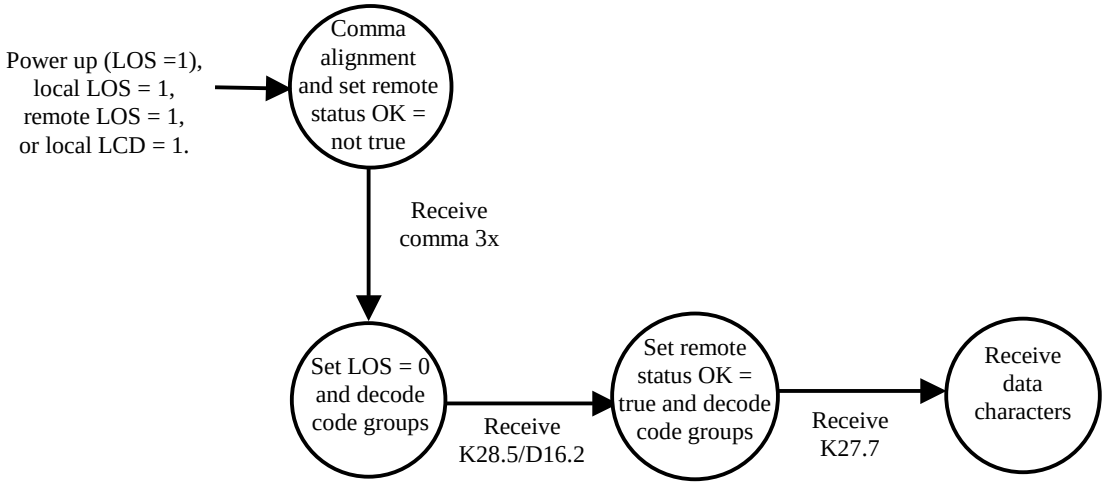

Figure 3 : Receive synchronization state diagram

(R49) At power up, a local LOS = 1, a remote LOS = 1 is received, or remote LCD = 1 is received; then the transmitter shall assume a positive running disparity and start transmitting K28.5/D5.6 code groups.

(R50) If the LOS = 0, the transmitter shall begin transmitting K28.5/D16.2 code groups starting when the current running disparity is negative.

(R51) The transmitter shall transmit a minimum of twenty-two consecutive K28.5/D16.2 code groups and if the remote status OK is true, then the transmitter shall transmit a K27.7 special character.

(R52) After the transmitter has transmitted a single K27.7 special character, the transmitter shall begin transmission of data characters.

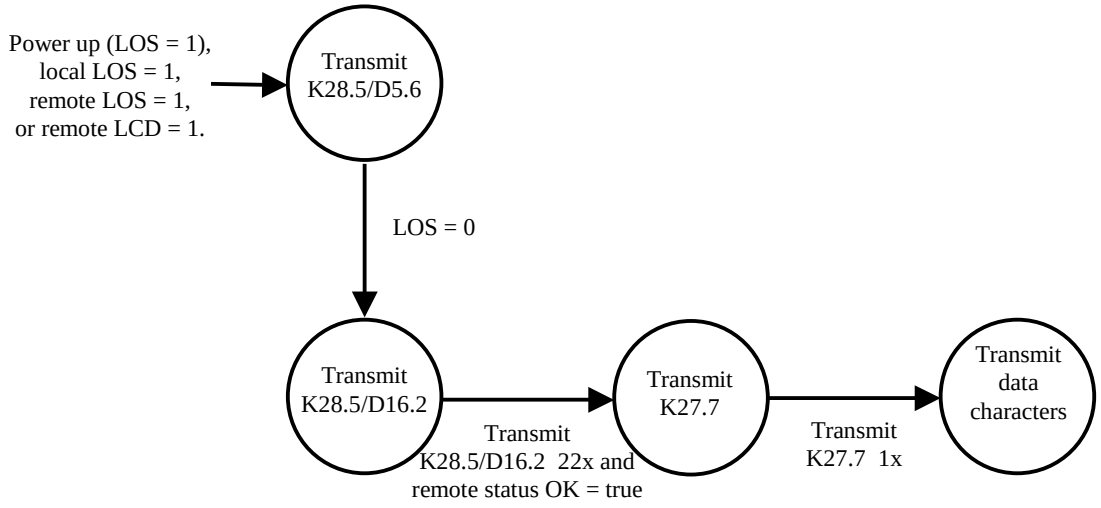

Figure 4 : Transmitter synchronization state diagram

3.4 Loss of synchronization

(R53) If the receiver after 4 ms has not completed synchronization: LOS = 0, remote status OK is true, and received a K27.7 special character; then the local LOS shall be set to 1 and the receiver and transmitter shall return to the start of synchronization.

(R54) At power up LOS shall be set to a 1.

3.5 Media dependent sublayer

The media dependent sublayer is defined by the TBI PMD. Two PMD's are defined in this specification for the 1000 Mbit/s Cell-Based Physical Layer.

3.5.1 Single-mode or multi-mode fiber

(R55) The single-mode or multi-mode fiber TBI PMD in this specification shall use the 1000BASE-X PMD, specified in Clause 38 of the 802.3 IEEE Standard, 2000 Edition [8].

3.5.2 Twisted pair copper cable

(R56) The category 6 twisted pair copper cabling TBI PMD in this specification shall use the PMD specified in TIA/EIA-854 [10].

4 Acronym List

AIS Alarm Indication Signal
BIP Bit Interleaved Parity
CEC Cell Error Control
CRC Cyclic Redundancy Code
DSS Distributed Sample Scrambler
EDC Error Detection Code
HEC Header Error Check
LCD Loss of Cell Delineation
LOM Loss Of Maintenance
LOS Loss Of Signal
MSB Most Significant Bit
OAM Operation And Maintenance
OCD Out of Cell Delineation
PCS Physical Coding Sublayer
PMA Physical Medium Attachment
PMD Physical Medium Dependent
PSN PL-OAM Sequence Number
PRBS Pseudo Random Binary Sequence
RDI Remote Defect Indication
REB Remote Error Blocks
TBI Ten Bit Interface
TC Transmission Convergence
TP Transmission Path

5 Normative References

The following references contain provisions that, through reference in this text, constitute provisions of this specification. At the time of publication, the editions indicated were valid. All references are subject to revision, and parties to agreements based on this specification are encouraged to investigate the possibility of applying the most recent editions of the references indicated below.

[1] ITU-T I.432.1 Recommendation, B-ISDN USER-NETWORK INTERFACE PHYSICAL LAYER SPECIFICATION - GENERAL CHARACTERISTICS - December, 1995.
[2] ITU-T I.432.2 Recommendation, B-ISDN USER-NETWORK INTERFACE PHYSICAL LAYER SPECIFICATION FOR 155 520 KBIT/S AND 622 080 KBIT/S - December, 1995.
[3] ITU-T I.361 Recommendation, B-ISDN ATM LAYER SPECIFICATION - 1993.
[4] ITU-T G.826 Recommendation, ERROR PERFORMANCE PARAMETERS AND OBJECTIVES FOR INTERNATIONAL, CONSTANT BIT RATE DIGITAL PATHS AT OR ABOVE THE PRIMARY RATE - July, 1995.
[5] ITU-T G.957 Recommendation, OPTICAL INTERFACES FOR EQUIPMENTS AND SYSTEMS RELATING TO THE SYNCHRONOUS DIGITAL HIERARCHY - July, 1995.
[6] ITU-T G.958 Recommendation, DIGITAL LINE SYSTEMS BASED ON THE SYNCHRONOUS DIGITAL HIERARCHY FOR USE ON OPTICAL FIBRE CABLES.
[7] AF/PHY/0046.000 ATM Forum specification, 622.080 Mbps Physical Layer Specification - January, 1996.
[8] 802.3 IEEE Standard, 2000 edition: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.
[9] TR/X3.18-1997 ANSI Technical Report (Fibre Channel – 10-bit Interface).
[10] TIA/EIA-854, A Full Duplex Ethernet Physical Layer Specification for 1000Mbits/s operating over Category 6 Balanced Twisted Pair Cabling..

APPENDIX I

Distributed Sample Descrambler Implementation Example

This Appendix does not form an integral part of this specification.

Acquisition of scrambler synchronisation

The conveyed bits are extracted by modulo addition of the predicted values for HEC_8 and HEC_7 from the received values. Scrambler synchronisation may for example be achieved by comparing the conveyed samples (U_{t-211}, U_{t+1}) at half cell intervals to the recursive descrambler sequence V_t (Figure I-1). In order to ensure the samples are compared to the recursive descrambler sequence at the same interval they were extracted from the source PRBS, the second sample $U_{(t+1)}$ (derived from HEC_7) is stored for 211 bits before it is used. Additionally, because both samples are applied to the recursive descrambler 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feedforward taps are chosen to generate a sequence that is advanced by 211 samples.

Figure I-1 illustrates a recursive descrambler implementation. Notation of sample values indicates the important sample values in each cell, time being referenced to the conveyed PRBS sample being received with HEC_8.

Acquisition state:
At time t:

– the receiver PRBS generator sample V_t is at the input to the lower D-type D_2;

– the source PRBS sample $S_t = U_{t-211}$ conveyed via HEC_8 is at input D_1;

– the sample previously stored at the output of the lower D-type is $Q_2 = V_{t-211}$

$$Xor2 = D_1 + Q_2 = U_{t-211} + V_{t-211}$$

At this time, the feedforward taps (constant correction vector) are applied to the descrambler if AND2 gate output is high, that is if $U_{t-211} \neq V_{t-211}$.

At time t+1:

– the receiver sample V_{t+1} is at the input to D_2;

– the sample $S_{t+1} = U_{t+1}$ is at the input to D_1.

These values are latched on the following clock edge such that:
At time t+2 through until t+212:

– $Xor1 = V_{t+1} + U_{t+1}$

At time t+212 :
At this time, the feedforward taps (constant correction vector) are applied to the descrambler if AND1 gate output is high, that is if $U_{t+1} \neq V_{t+1}$.
At time t+213 = L + t–211 (L being the duration of a cell):

– $Q_2 = V_{t+213} = V_{t-211+L}$ (held until the next cell cycle).

Verification of descrambler synchronisation

In this state the conveyed samples (U_{t-211},U_{t+1}) are extracted in the same way as during the Acquisition state, but the feedforward taps are no longer applied. Instead for each cell received with no error detected in bits HEC 1 to 6, the conveyed samples (U_{t-211},U_{t+1}) are compared to the corresponding bits (V_{t-211},V_{t+1}) generated locally by the descrambler. Each time two correct predictions are made the confidence counter is incremented, else it will decrement.

Steady state operation (synchronised scrambler)

In this state the descrambler is assumed to be synchronised and feedforward taps are no longer applied. Instead, the descrambler samples (V_{t-211},V_{t+1}) are added by modulo 2 addition to the first two bits of the received HEC byte in order to regenerate the values of HEC8 and HEC7 bits. Therefore bits HEC8 and HEC7 can both be returned to normal use for error detection and error correction properties.

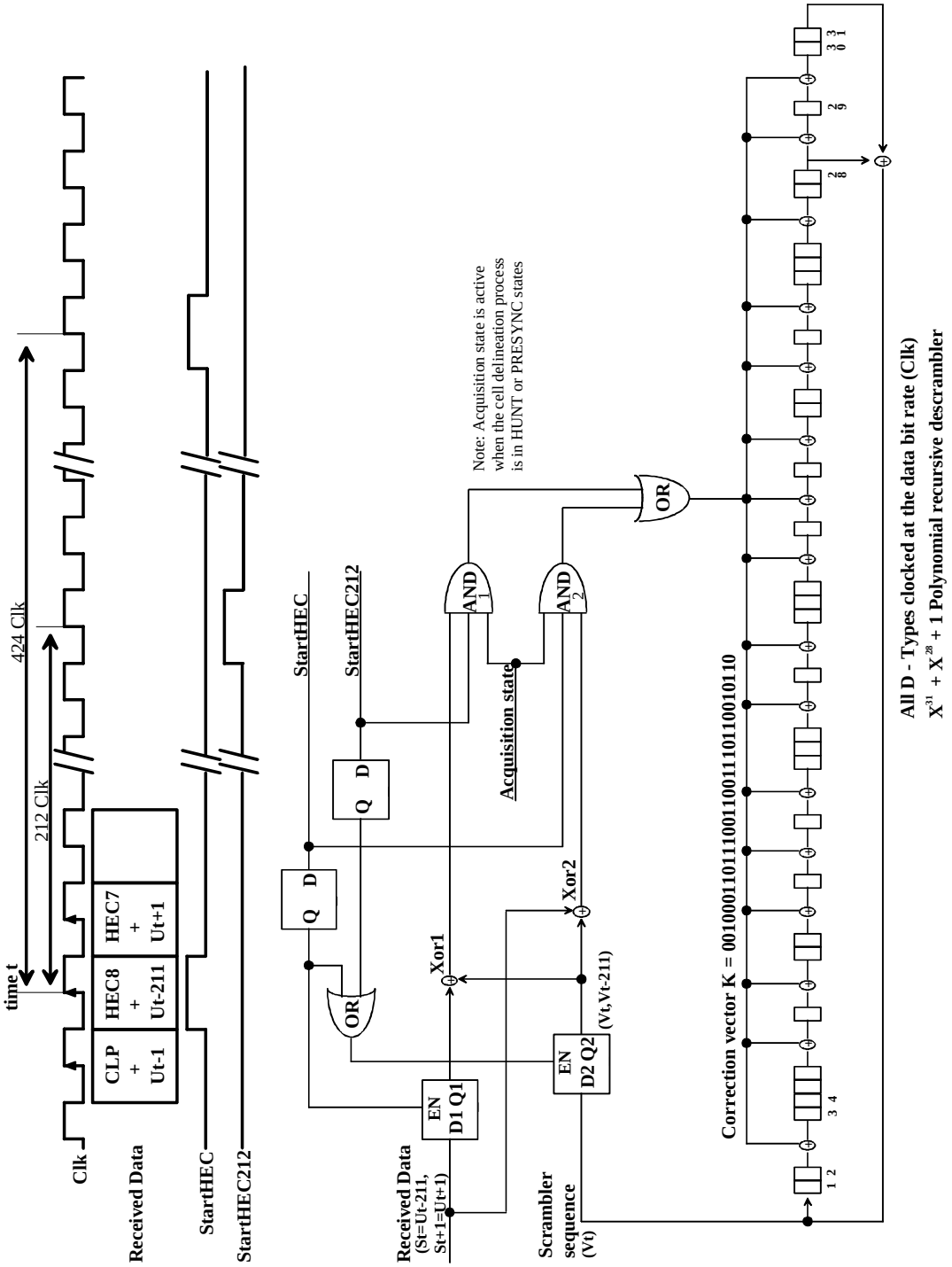

Figure I-1 : Example of descrambler implementation

APPENDIX II

Test Patterns

This Appendix does not form an integral part of this specification.

The example of operation described in this appendix is based on the transmission of 17 consecutive idle cells generated by the Cell-Based TC sublayer described in section 2. The transmitter operation is described in II 1 of this appendix and the receiver operation is described in II 2 of this appendix.

Notations:

- The content of an ATM cell is presented in the following format : H1 H2 H3 H4 HEC P1 ..... P48. The bytes H1 to H4 correspond to the cell header while the bytes P1 to P48 correspond to the cell payload. Each byte is given in hex value (hXX),
- The reference of time is noted **t** (both in the transmitter and in the receiver),
- U(t+x) is the state of the scrambler in the transmitter at time t+x. It is noted either as a 31 bits vector or as an hex value (example : U(t+x) = 00000000111111110000000001111111 = h7F00FF00),
- V(t+x) is the state of the descrambler in the receiver at time t+x. It is noted either as a 31 bits vector or as an hex value,
- U_{t+x} is the output of the scrambler in the transmitter at time t+x,
- V_{t+x} is the output of the descrambler in the receiver at time t+x.

The content of an idle cell (prior to scrambling and HEC calculation) is :

```
00 00 00 01 xx 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A
6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A
```

II 1 Transmitter operation

The time reference in the transmitter is defined as the time when the first bit of the HEC field of the first cell is generated, coincident with the scrambler state U(t). So t corresponds to the generation of the first HEC_8 bit in the transmitter (Figure II-1).

At time t the scrambler in the transmitter is in a random state. If U(t) = h3ECFEDE8 then $U_t = 1$.

II 1.1 Cell scrambling

The scrambler sequence is added (modulo 2) bit by bit to the whole cell, except the HEC field, but the scrambler in the transmitter is not stopped during that time. This operation is represented in Figure II-1, as well as the scrambler state at time t.

When U(t) = h3ECFEDE8 then U(t-32) = h0ABB8F39 and $U_{t-32} = 1$.

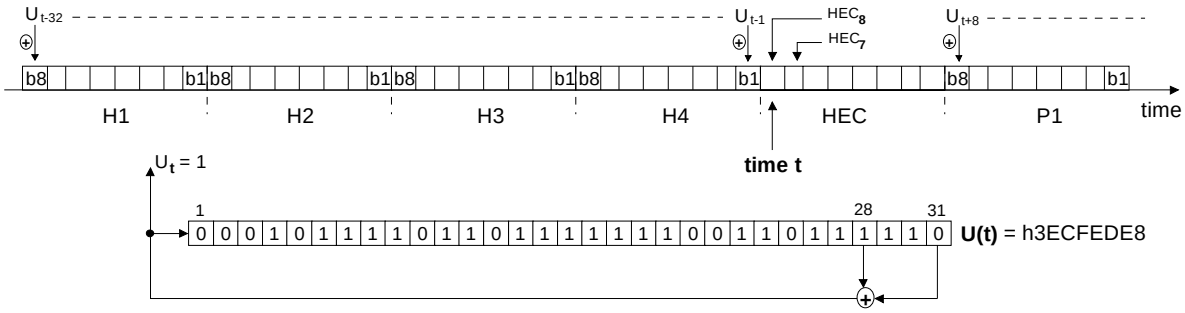

Figure II-1 : Scrambling operation and scrambler initial state

After the scrambling is performed, the 17 idle cells become :

```
Cell 1:
BE CF ED E9 xx 0B 6F 32 5E B8 35 59 4E EB 27 3E 6B 7C 25 82 79 22 0B 3B 78 7C BD D9 6F
2A BE 3C 34 E6 87 A3 3F BD 6D 6D 9C B4 14 1A EA 31 71 83 6F 6D E3 28 30
Cell 2:
77 86 A1 12 xx 0D 39 74 32 D1 FD B3 50 A4 38 4B B3 13 EC 34 4F 01 03 34 76 0A 2D 37 94
AE 91 0E 7B AC 2A E3 55 82 E3 EB EB 33 E1 71 7D 41 CD ED 36 87 5D 11 1D
Cell 3:
09 19 41 9F xx CC F0 BF 57 4E F2 93 C2 6A D4 03 BA 60 F0 24 CA D6 FA 1D 20 DA 4D F0 54
08 5C FD F0 8D 6E 3C F1 D4 27 AE E6 F2 2D AB BA DE 99 F4 C0 4C B4 BD 9C
Cell 4:
20 50 D0 8F xx C6 C3 92 BB F9 A6 16 D0 71 35 58 BF E9 27 22 99 58 24 74 BF 2A 17 BA 94
ED 4C C4 7F 16 4D D7 17 50 5E C7 43 BD 49 E2 A4 B6 15 F7 1A 15 6C 87 8D
Cell 5:
0E 63 05 BF xx 9C 3A F8 30 E3 C2 6B 77 E3 BA 79 89 E4 CB 73 95 9D 39 C6 6A F1 F7 F2 62
E4 88 DA F3 99 84 02 C6 B3 50 31 FE 4B BB 64 00 34 D8 90 1B 3C 20 39 9D
Cell 6:
C8 31 98 92 xx 10 D2 7D 7B 34 9B 35 5D 38 9D 27 71 E0 F0 21 E5 D6 FA 45 8E DA 48 CB E8
08 05 31 48 88 41 6E 01 8C 8C 24 03 C9 C2 10 23 17 BD 3A 6F 4C B1 CA 32
Cell 7:
20 0D 45 33 xx A4 B3 2A E7 1A 4C E3 A7 88 4F E5 2F 8C 79 80 BF C7 73 12 9B E1 CF 14 91
C7 77 78 27 E1 81 6A 29 C3 0C 6E D7 AE C6 28 CD A9 F6 C5 59 D4 99 C7 36
Cell 8:
92 DD 8F 71 xx 09 83 8A FC 93 27 A2 28 0C 2D 7E C8 C2 95 09 05 B4 62 9A 48 36 F4 88 0B
1A B9 88 BF 86 F3 82 9F 7A C7 34 D1 41 E5 3C AE 85 81 AB AD 4B 01 F5 96
Cell 9:
54 6E C0 3C xx 5B E9 CF 55 11 57 73 E3 2F C1 C1 EC BB 87 85 0A D7 6F 42 A0 C0 32 B7 55
9B 56 03 EA 9B D4 21 64 92 F2 4C 98 12 D8 48 A9 10 2C 03 DB 3A 80 22 1D
Cell 10:
AF 70 17 94 xx 8B 3C 1B A7 BD A1 95 2C B9 42 60 8A FE BA D1 A2 0E C0 A1 7C E9 93 4D 2F
52 0A 50 B3 9C A9 B2 46 EB D0 58 FB 72 BD 26 59 D6 B0 31 36 DE 7B 69 18
Cell 11:
29 32 31 C7 xx 2D 15 8B FC 93 6B B0 28 08 74 7A C8 8F B7 41 01 FC 02 8A 04 20 35 AC 52
5B 29 85 99 1C D3 4A BB EC 8A 26 D1 09 AE 38 AA 91 A7 E3 E4 21 29 E1 92
Cell 12:
22 BF A8 73 xx EF BD A8 5F 3C B9 CD 55 AA F7 57 E9 E2 83 C9 55 F5 23 1F EC A0 6F D9 0B
5E 3A 3A BB 47 CF C6 DA EB 7B F8 03 79 50 68 29 7F BE 4A DD 1C 80 20 73
Cell 13:
83 70 35 AA xx 89 5B 8F 17 9F 17 F7 4E D7 48 82 68 C2 01 3A 45 BC 09 C8 C8 A0 97 05 03
50 46 42 2B BC F0 BE F4 AE F2 8A BB AA D5 A6 D5 E0 E9 38 ED D7 59 E7 1E
Cell 14:
A9 5F CD A2 xx 29 2B 11 90 D8 FF 22 34 26 14 7F 32 35 77 15 5F 25 87 67 54 0B 60 A3 F0
B8 D3 60 F2 E4 88 D6 D3 99 84 D8 86 B3 5C 21 7E 4B 62 4D 00 38 F8 52 1B
Cell 15:
8C 07 F7 FA xx 1A FA 20 5D 82 4E 5D 7B 38 61 75 5D EE CD A7 7D 29 59 21 30 DF 38 49 74
55 EC 1D B5 ED 01 F8 2D 12 04 6A 93 1C 56 64 0F E5 D2 90 F9 8E 94 36 73
```

```
Cell 16:
86 19 79 AA xx CF 03 8A 6B 76 27 AA 79 96 2D EB 72 56 9D 79 D9 DC F5 76 36 6E A5 97 12
2F 0A 47 1E B6 A8 E7 CE 1F C7 AB 65 DB ED F8 8E 11 1C 61 E5 2B E6 C5 80
Cell 17:
9B D3 A1 7D xx F7 3F 5B D6 85 93 12 DD 4A 0F 10 76 2C F7 3F 96 8E 85 9E 5D ED 4A C1 7D
16 21 8D 33 56 43 D1 4B D0 A2 AE 32 B3 77 A7 56 49 8D 23 D0 13 D0 62 B9
```

II 1.2 HEC generation

The HEC value is computed on the scrambled header and the pattern h55 is added to the HEC field by modulo 2 addition.
For the first cell : HEC (`BE CF ED E9`) = hAD xor h55 = hF8.
The HEC field of each cell after this operation is given in the following table :

Table II-1 : HEC field

Cell	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
HEC	F8	00	F1	A1	9C	7B	89	B4	41	C6	BD	F4	DE	0C	0D	C8	62

II 1.3 Addition of scrambler samples

The last operation consists in modifying bits HEC_8 and HEC_7 of each cell to convey the two scrambler samples.
For the first cell : $HEC_8 = HEC_8$ xor U_{t-211} and $HEC_7 = HEC_7$ xor U_{t+1},
For the second cell : $HEC_8 = HEC_8$ xor U_{t+213} and $HEC_7 = HEC_7$ xor U_{t+425},
For the third cell : $HEC_8 = HEC_8$ xor U_{t+637} and $HEC_7 = HEC_7$ xor U_{t+849},
.....
Consequently the final value of the HEC field of each cell is given in the following table :

Table II-2 : Final HEC field

Cell	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
HEC	78	80	F1	61	5C	7B	49	34	01	46	FD	B4	DE	CC	4D	08	62

II 1.4 Transmitted bytes

Important note: the transmitter operation has been described in three separate steps (II 1.1, II 1.2, and II 1.3) but as these three operations are linear they can be done at the same time (especially operations II 1.1 and II 1.3 which are both related to the scrambler output).

As a result of the operations described in II 1.1, II 1.2, and II 1.3 the resulting output is given below. Bytes are transmitted from left to right. In each byte the MSB (Most Significant Bit) is transmitted first. The HEC byte of each cell is highlighted.

```
BE CF ED E9 78 0B 6F 32 5E B8 35 59 4E EB 27 3E 6B 7C 25 82 79 22 0B 3B 78 7C BD D9 6F
2A BE 3C 34 E6 87 A3 3F BD 6D 6D 9C B4 14 1A EA 31 71 83 6F 6D E3 28 30 77 86 A1 12 80
0D 39 74 32 D1 FD B3 50 A4 38 4B B3 13 EC 34 4F 01 03 34 76 0A 2D 37 94 AE 91 0E 7B AC
2A E3 55 82 E3 EB EB 33 E1 71 7D 41 CD ED 36 87 5D 11 1D 09 19 41 9F F1 CC F0 BF 57 4E
F2 93 C2 6A D4 03 BA 60 F0 24 CA D6 FA 1D 20 DA 4D F0 54 08 5C FD F0 8D 6E 3C F1 D4 27
AE E6 F2 2D AB BA DE 99 F4 C0 4C B4 BD 9C 20 50 D0 8F 61 C6 C3 92 BB F9 A6 16 D0 71 35
58 BF E9 27 22 99 58 24 74 BF 2A 17 BA 94 ED 4C C4 7F 16 4D D7 17 50 5E C7 43 BD 49 E2
A4 B6 15 F7 1A 15 6C 87 8D ... (cells 5 to 16) ...

Last cell :
9B D3 A1 7D 62 F7 3F 5B D6 85 93 12 DD 4A 0F 10 76 2C F7 3F 96 8E 85 9E 5D ED 4A C1 7D
16 21 8D 33 56 43 D1 4B D0 A2 AE 32 B3 77 A7 56 49 8D 23 D0 13 D0 62 B9
```

II 2 Receiver operation

At start up the cell delineation process is in HUNT state and the descrambler process is in Acquisition state (C=0).

During the HUNT state, the HEC check is done only on the last six bits of the HEC field (bits HEC6 to HEC1). As soon as a correct HEC is found the cell delineation process enters the PRESYNC state (where the HEC check is still done on 6 bits). During the PRESYNC state, the descrambler is in Acquisition state and the two conveyed samples (U_{t-211}, U_{t+1}) are extracted and used for descrambler synchronisation.

The first correct HEC is detected upon reception of the following bytes : `BE CF ED E9 78`, because : HEC (`BE CF ED E9`) = hAD, this value is compared to (h78 xor h55 = h2D) and the last six bits are the same.

The time reference in the receiver is defined as the time when the first bit of the HEC field of the first cell is received, coincident with the descrambler state V(t). At time t the descrambler is in a random state. If V(t) = h2477F94D then $V_t = 0$.

II 2.1 Acquisition state

During this state the conveyed samples are extracted by modulo addition between the received HEC value and the predicted HEC value :

Cell 1 : received value = h78
predicted value = (HEC (`BE CF ED E9`) = hAD) xor h55 = hF8
comparison between these two values : h78 xor hF8 = h80, so $U_{t-211} = 1$ and = $U_{t+1} = 0$.

Cell 2 : received value = h80
predicted value = (HEC (`77 86 A1 12`) = h55) xor H55 = h00
comparison between these two values : h80 xor h00 = h80, so $U_{t+213} = 1$ and = $U_{t+425} = 0$.

The conveyed samples are used for descrambler synchronisation, as explained in Appendix I. Every 212 bits the received sample U_{t+x} is compared to the corresponding bit V_{t+x} generated by the descrambler. If these two samples are not identical a constant correction vector (K= h34DCCEC4) is applied :
at time t : $V_{t-211} = 0$ is compared to $U_{t-211} = 1$→ the correction vector K is applied,
at time t+212 : $V_{t+1} = 0$ is compared to $U_{t+1} = 0$ → the correction vector K is not applied,
at time t+424 : $V_{t+213} = 0$ is compared to $U_{t+213} = 1$→ the correction vector K is applied,...
The following table indicates the descrambler state at the times when the samples are compared and when the correction vector is potentially applied.

Table II-3 : Descrambler state

Time (t+x)	V(t+x) (bits 1 to 31)	V_{t+x}	Comparison between :		Cor.
			descrambler	scrambler	
-211	0001110111110000110111000101001	0	-	-	-
0	1011001010011111111011100010010	0	V_{t-211}=0	U_{t-211}=1	yes
1	0111101000111100110011000011111	0	-	-	-
212	0100110000000100100000010110011	1	V_{t+1}=0	U_{t+1}=0	no
213	1010011000000010010000001011001	0	-	-	-
424	0110110000000100000001011111010	1	V_{t+213}=0	U_{t+213}=1	yes
425	1001010101110001001110011101011	0	-	-	-
636	0011100010000011101001000010110	0	V_{t+425}=0	U_{t+425}=0	no
637	0001110001000001110100100001011	0	-	-	-
848	1011101000111001001001100110010	0	V_{t+637}=0	U_{t+637}=0	no
849	0101110100011100100100110011001	0	-	-	-
1060	0100111011010100110000111000111	1	V_{t+849}=0	U_{t+849}=0	no
1061	1010011101101010011000011100011	1	-	-	-

1272	01110001000001110111011011101 00	0	$V_{t+1061}=1$	$U_{t+1061}=1$	no
1273	00111000100000111011101101110 10	1	-	-	-
1484	11100101110101110111111001000 101	1	$V_{t+1273}=1$	$U_{t+1273}=1$	no
1485	11110010111010111011111001001 00	0	-	-	-
1696	11111100010101001011101010111 11	0	$V_{t+1485}=0$	$U_{t+1485}=1$	yes
1697	01011101010110010110011001110 01	0	-	-	-
1908	11100011011000100100001110011 10	1	$V_{t+1697}=0$	$U_{t+1697}=1$	yes
1909	11010010110000100001101011100 01	1	-	-	-
2120	10001010111011001101011010010 10	1	$V_{t+1909}=1$	$U_{t+1909}=0$	yes
2121	11100110000001010101000001100 11	1	-	-	-
2332	10001111111001011101101100101 11	1	$V_{t+2121}=1$	$U_{t+2121}=0$	yes
2333	11100100100000011101011010111 01	0	-	-	-
2544	01110011100010010011000110110 00	1	$V_{t+2333}=0$	$U_{t+2333}=1$	yes
2545	10011010101101111010001111110 10	1	-	-	-
2756	01001110110000011010111000001 10	0	$V_{t+2545}=1$	$U_{t+2545}=1$	no
2757	00100111011000001101011100000 11	1	-	-	-
2968	10110111011001011011111110001 11	1	$V_{t+2757}=1$	$U_{t+2757}=1$	no
2969	11011011101100101101111111000 11	1	-	-	-
3180	11000100101001001001010110001 01	1	$V_{t+2969}=1$	$U_{t+2969}=0$	yes
3181	11000001001000010111000111101 00	0	-	-	-
3392	00100111010011110010111110011 11	0	$V_{t+3181}=0$	$U_{t+3181}=0$	no
3393	00010011101001111001011111001 11	1	-	-	-
3604	01101000010010100111100000011 10	1	$V_{t+3393}=1$	$U_{t+3393}=1$	no
3605	10110100001001010011110000001 11	1	-	-	-
3816	01010000001110011101010000100 01	1	$V_{t+3605}=1$	$U_{t+3605}=1$	no
3817	10101000000111001110101000010 00	1	-	-	-
4028	01100101011111110000111110101 10	0	$V_{t+3817}=1$	$U_{t+3817}=0$	yes
4029	00010001110011001011110011111 01	0	-	-	-
4240	11001111101101010001100110010 01	0	$V_{t+4029}=0$	$U_{t+4029}=0$	no
4241	01100111110110101000110011001 00	0	-	-	-
4452	01100001001011001011110000001 01	1	$V_{t+4241}=0$	$U_{t+4241}=1$	yes
4453	10010011111001010110010100101 00	0	-	-	-
4664	11011011000010011101010001111 11	0	$V_{t+4453}=0$	$U_{t+4453}=0$	no
4665	01101101100001001110101000111 11	0	-	-	-
4876	00001110000101110111101110101 10	1	$V_{t+4665}=0$	$U_{t+4665}=1$	yes
4877	10100100011110001000011011000 11	1	-	-	-
5088	11110010101101001100000011101 10	0	$V_{t+4877}=1$	$U_{t+4877}=0$	yes
5089	01011010001010010101101101011 01	0	-	-	-
5300	10010110100000001101101100011 01	0	$V_{t+5089}=0$	$U_{t+5089}=0$	no
5301	01001011010000000110110110001 10	0	-	-	-
5512	00011111111000001110110000011 11	0	$V_{t+5301}=0$	$U_{t+5301}=1$	yes
5513	00101100100000110100110100100 01	1	-	-	-
5724	00100000010010101101100010110 00	1	$V_{t+5513}=1$	$U_{t+5513}=1$	no
5725	10010000001001010110110001011 00	1	-	-	-
5936	00110111100100110001000000000 00	0	$V_{t+5725}=1$	$U_{t+5725}=0$	yes
5937	00111000101110101011001100101 10	0	-	-	-
6148	01011001001000011111101000011 11	0	$V_{t+5937}=0$	$U_{t+5937}=1$	yes
6149	00001111111100011110001100010 01	1	-	-	-
6360	11010101100111101001100001100 00	0	$V_{t+6149}=1$	$U_{t+6149}=1$	no
6361	01101010110011110100110000110 00	1	-	-	-
6572	01101010001000011110101111111 11	0	$V_{t+6361}=1$	$U_{t+6361}=1$	no
6573	00110101000100001111010111111 11	0	-	-	-

Note: In this example the correction vector is applied 15 times. For each acquisition process, the number of times the correction vector is applied only depends on the transmit scrambler and the receive descrambler initial states which are random. For 16 consecutive cells received with no error detected in HEC bits 1 to 6, the number of times the correction vector is applied ranges from 0 to 31 (0 corresponds to the unlikely case where the transmit scrambler and the receive descrambler are synchronised at start-up)

During the Acquisition state, each time a cell is received with no error detected in HEC bits 1 to 6, the confidence counter is incremented (C=C+1). Therefore at time t+6572 (cell number 17) the confidence counter has reached the value 16 and the descrambler process enters the Verification state.

II 2.2 Verification state

When entering the Verification state, the descrambler in the receiver is assumed to be synchronised, because the 31 conveyed samples received during the Acquisition state are sufficient to insure descrambler synchronisation (this process is deterministic and does not depend on the transmit scrambler and receive descrambler initial states). However because the HEC check during the Acquisition state is performed only on the last six bits, undetected errors may have occurred in the conveyed samples (bits HEC_8 and HEC_7) resulting in incorrect descrambler synchronisation. For this reason the Verification process tests for a couple of cells that the PRBS bits generated locally by the descrambler (V_{t-211},V_{t+1}) are identical to the expected ones (U_{t-211},U_{t+1}).

During the Verification state the conveyed samples (U_{t-211},U_{t+1}) are extracted in the same way as during the Acquisition state. Then they are compared to the PRBS bits generated locally (V_{t-211},V_{t+1}) but feedforward taps are no longer applied. Instead when two correct predictions are made the confidence counter is incremented, else it will decrement.

At time t+6752 the first bit of cell 17 is received. At this time the descrambler state is h418CAFEA and the descrambler process has just entered the Verification state.

Received header for cell 17 : 9B D3 A1 7D 62 (HEC value = h62),
Predicted HEC value = HEC (9B D3 A1 7D) xor h55 = h37 xor h55 = h62,
Comparison between received HEC and predicted HEC : h62 xor h62 = h00, so $U_{t+6573} = 0$ and = $U_{t+6785} = 0$.

These received samples are compared to the corresponding bits generated locally by the descrambler ($V_{t+6573} = 0$, $V_{t+6785} = 0$). As they are identical the confidence counter is incremented (C=17). This verification process is repeated for the following cells (cells 18 to 24) until the confidence counter reaches the value of 24 and the descrambler process moves to the Steady state.

Note :
It is easy to verify that the descrambler is actually correctly synchronised when entering the Verification state :

at time t+6752 the descrambler state is h418CAFEA, so the bytes generated by the descrambler from time t+6752 are :

```
9B D3 A1 7C xx 9D 55 31 BC EF F9 78 B7 20 65 7A 1C 46 9D 55 FC E4 EF F4 37 87 20 AB 17
7C 4B E7 59 3C 29 BB 21 BA C8 C4 58 D9 1D CD 3C 23 E7 49 BA 79 BA 08 D3
```

at time t+6752 (beginning of cell 17) the received bytes are :

```
9B D3 A1 7D 62 F7 3F 5B D6 85 93 12 DD 4A 0F 10 76 2C F7 3F 96 8E 85 9E 5D ED 4A C1 7D
16 21 8D 33 56 43 D1 4B D0 A2 AE 32 B3 77 A7 56 49 8D 23 D0 13 D0 62 B9
```

after modulo addition the result is :

```
00 00 00 01 xx 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A
6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A 6A
```

II 2.3 Steady state operation

In this state the descrambler is assumed to be synchronised. The PRBS generated locally by the descrambler is used to descramble both the header and the payload of the received cells. The conveyed samples (U_{t-211},U_{t+1}) are no longer extracted, instead they are descrambled by modulo addition with the corresponding descrambler bits (V_{t-211},V_{t+1}).

During this state the HEC check is performed by using the full eight bits of the HEC field thus enabling multiple bit error detection and single bit error correction. Cells with correct HEC (or cell headers with single bit error which are corrected) are passed to the ATM layer.

When the HEC check indicates a non-zero syndrome with error bits confined to HEC_8 and HEC_7 the confidence counter will decrement, else it is incremented (the upper limit of the confidence counter is 24).

II 2.4 Parallel implementation

The descrambler behaviour described in II 2.1, II 2.2, and II 2.3 of this appendix does not depend on the implementation of the DSS (serial or parallel). Nevertheless, in parallel implementation of the DSS, to receive data words (of 8, 16, or 32 bits) instead of a bit stream requires slight modifications in the application of the correction vector.

Example:
If the DSS implementation is in parallel with the 8 bit data word. The clock edges occur at time t, t+8,..., t+1904, t+1912,.... Taking the same values as in II 2.1 :

- From a serial description :

  V(t+1908) = h`39C246C7` (correction vector K= h`34DCCEC4` is applied)
  V(t+1909) = h`4758434B`
  V(t+1912) = h`3AC21A5F`
  V(t+1913) = h`758434BF`

- From a 8 bits parallel implementation :
  The correction vector K can not be applied at time t+1908 because this time is not coincident with a clock edge, so a modified correction vector K' will be applied at the next clock edge t+1912 (that is 4 bits later).

The determination of K' is deduced from K by a 4 bits shift using the same polynomial as the scrambler (1+x^28+x^31). So K'= h`4DCCEC42`.