Note

This is a transcription of a photocopy of the original DBRI data sheet, which I've been otherwise unable to locate in electronic form.

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Pin Information

Tables 1-5 list the location, name, and type for each pin on the DBRI.

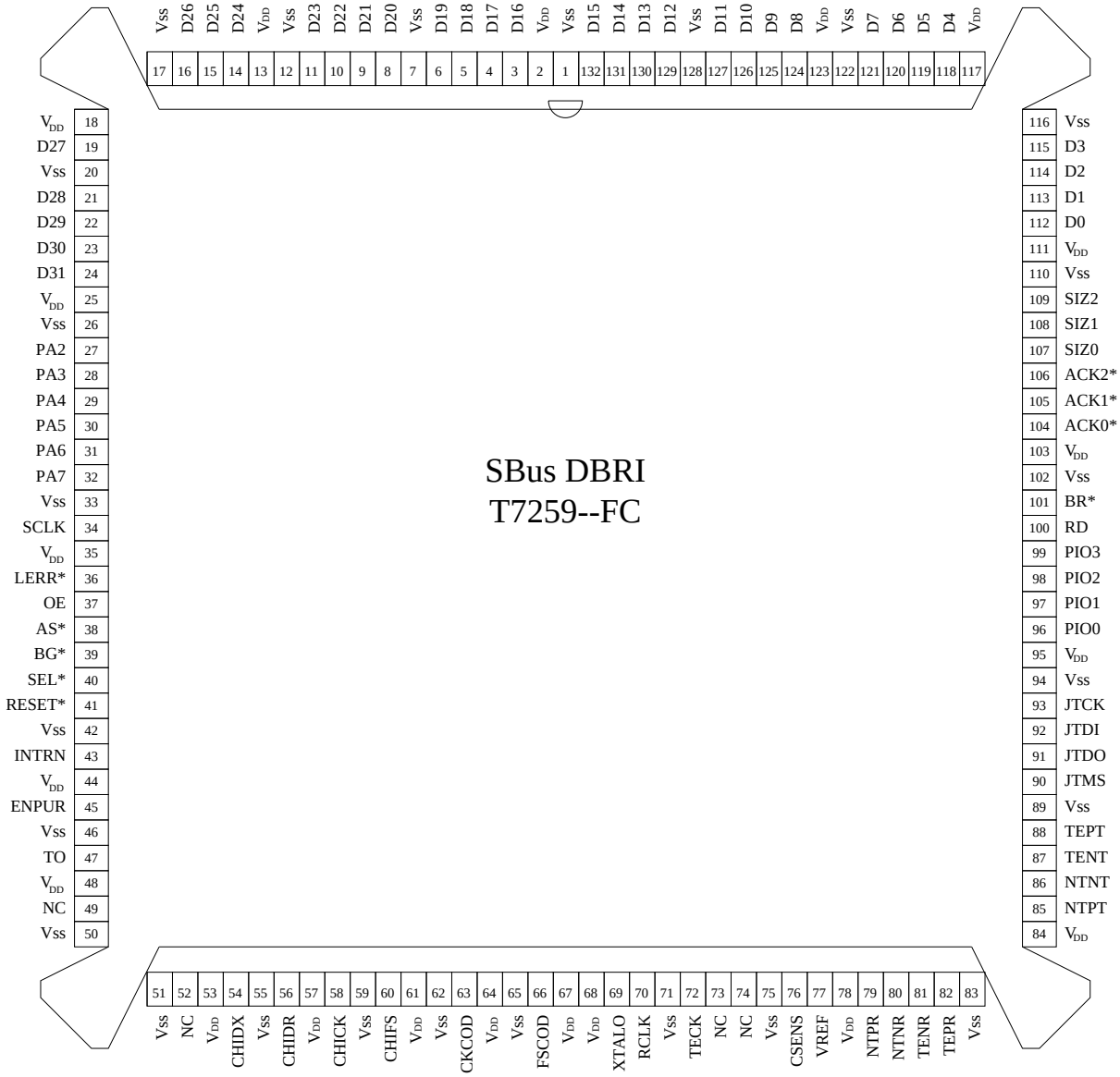

Figure 1. Pin Diagram

Good power supply bypass techniques should be followed with this device. One technique is to bypass each power supply pin to ground as close to the device as possible with 0.1 µF capacitors. Use of ground and power planes may reduce the required number of capacitors. However, in every application, it is recommended that pin 78 be separately bypassed since this pin is the primary power pin for the analog receiver.

Table 1. Pin Descriptions (Power Supply Pins)

Pin	Symbol	Type[1]	Name/Function
2, 13, 18, 25, 35, 44, 48, 53, 57, 61, 64, 67, 68, 78, 84, 95, 103, 111, 117, 123	V_{DD}	P	**Power.** 5V±5% TNRT
1, 7, 12, 17, 20, 26, 33, 42, 46, 50, 51, 55, 59, 62, 65, 71, 75, 83, 89, 94, 102, 110, 116, 122, 128	V_{SS}	G	**Ground.**
76	CSENS	A	**Current Sense.** Connect CSENS to V_{SS} via 11.3 kohm ± 0.1% resistor.
77	V_{REF}	A	**Voltage Sense.** Connect V_{REF} to V_{DD} via 27.4 kohm ± 0.1% resistor.

[1] I=input, O=output, B=bidirectional, A=analog, P=power, G=ground.

Table 2. Pin Descriptions (Serial Interface Pins)

Pin	Symbol	Type[1]	Name/Function
79	NTPR	AI	**N Receiver Positive Side.**
80	N	AI	**NT Receiver Negative Side.**
81	TENR	AI	**TE Receiver Negative Side.**
82	TEPR	AI	**TE Receiver Positive Side.**
85	NTPT	AO	**NT Transmit Positive Side.**
86	NTNT	AO	**NT Transmit Negative Side.**
87	TENT	AO	**TE Transmit Negative Side.**
88	TEPT	AO	**TE Transmit Positive Side.**
72	TECK	O	**4 kHz Digital Phase-Locked Loop (DPLL) for External Analog Phase-Locked Loop (APLL).** TDOEL
54	CHIDX	B	**Concentration Highway Transmit Data.** IZ
56	CHIDR	B	**Concentration Highway Receive Data.**
58	CHICK	B	**Concentration Highway Clock.**
60	CHIFS	B	**Concentration Highway Frame Strobe.**

[1] I=input, O=output, B=bidirectional, A=analog, P=power, G=ground.

Table 3. Pin Descriptions (SBus Pins) (See Sun SBus Specification A.2)

Pin	Symbol	Type[1]	Name/Function
27-32	PA[2-7]	I	**Physical Address.**
112-115, 118-121	D[0-3, 4-7]	B	**Data.**
124-127, 129-132	D[8-11, 12-15]	B	**Data.**
3-6	D[16-19]	B	**Data.**
8-11, 14-16	D[20-23, 24-26]	B	**Data.**
19, 21-24	D[27, 28-31]	B	**Data.**
107-109	S[0-2]	B	**Size.**
100	RD	B	**Transfer Direction.**
101	BR*	O	**Bus Request.**
104-106	ACK[0-2]*	B	**Transfer Acknowledge.**
36	LERR*	I	**Late Data Error.**
38	AS*	I	**Address Strobe.**
39	BG*	I	**Bus Grant.**
40	S*	I	**Chip Select.**
41	RESET*	I	**Reset.** Approximately 100 system clock cycles after the rising edge of the reset, the DBRI has identification code (ID code) available. Reset causes the sanity timer to expire, forces the CHI into high-impedance state, and drops communication on the TE interface.
43	INTR*	O	**Interrupt.**Open drain.

[1] I=input, O=output, B=bidirectional, A=analog, P=power, G=ground.

Table 4. Pin Descriptions (JTAG and Clock Pins)

Pin	Symbol	Type[1]	Name/Function
90	JTMS	I	**JTAG TAP Control In.**
91	J	O	**JTAG Serial Data Out.**
92	JTDI	I	**JTAG Serial Data In.**
93	JTCK	I	**JTAG TAP Clock.**
34	SCLK	I	**System Clock.** 16.67 MHz to 25 MHz.
69	XTALO	AO	**Crystal Out Feedback.**
70	RCLK	I	**Reference Clock/Crystal Oscillator Input.**
63	CKCOD	O	**Codec Clock.** The DBRI provides a 1.536 MHz or 2.048 MHz clock derived by counting the DPLL. CKCOD can be disabled (held high) when it is not needed.
66	FSCOD	O	**Codec Frame Sync.** EThe rising and falling edges of FSCOD are individually programmed to occur a given number of DPLL cycles after the start of a CHI frame. This allows FSCOD to look like either an active-high or active-low pulse, with a duration of any number of DPLL clock cycles, positioned at any DPLL clock cycle boundary within the CHI frame. FSCOD can be disabled (held high) when it is not needed by programming the rising and falling edges to occur at the same time.

[1] I=input, O=output, B=bidirectional, A=analog, P=power, G=ground.

Table 5. Pin Descriptions (Miscellaneous Pins)

Pin	Symbol	Type[1]	Name/Function
37	O	I	**Output Enable.** When high, the chip outputs are enabled. When low, the chip outputs are disabled (high impedance) except XTALO and JTDO.
45	ENPUR	I	**Powerup Reset Enable Pin.** Active-high. This pin should be tied to VDD.
47	TO	O	**Sanity Timer Time-Out.** This active-low output indicated that the DBRI's 8.192 second sanity timer has expired. After reset, TO remains low until the F-bit in REG0 is cleared. After the F-bit is cleared, TO is high unless the sanity timer times out. The sanity timer is reset every time the DBRI executes a command or a register is accessed Tin slave mode (including information code). E
96-99	PIO[0-3]	B	**General-Purpose Parallel I/O.**

[1] I=input, O=output, B=bidirectional, A=analog, P=power, G=ground.

Application Overview

The DBRI is intended for use in desktop equipment such as a PC, PC plug-in card, workstation (WS), or video box (VB), and provides a basic rate ISDN connection to the network. In addition, the PC/WS/VB can terminate a desktop ISDN connection in either point-to-point or point-to-multipoint mode. At the highest level, the DBRI is an integrated circuit with four interfaces to the external world: an ISDN NT interface to support a desktop passive bus connected to an ISDN telephone and perhaps other ISDN devices; an ISDN TE interface to connect to the ISDN network; a DMA interface to system memory; and a concentration highway interface (CHI) connecting to external devices. The DBRI serves as a conduit for communication between these points. In addition, the DBRI supports various types of external (voice and/or video) codecs by supplying a programmable FS signal and clock.

In the simplest application, the DBRI terminates an ISDN telephone. In this configuration, the PC/WS can be used to enhance the usefulness and usability of the desktop telephone.

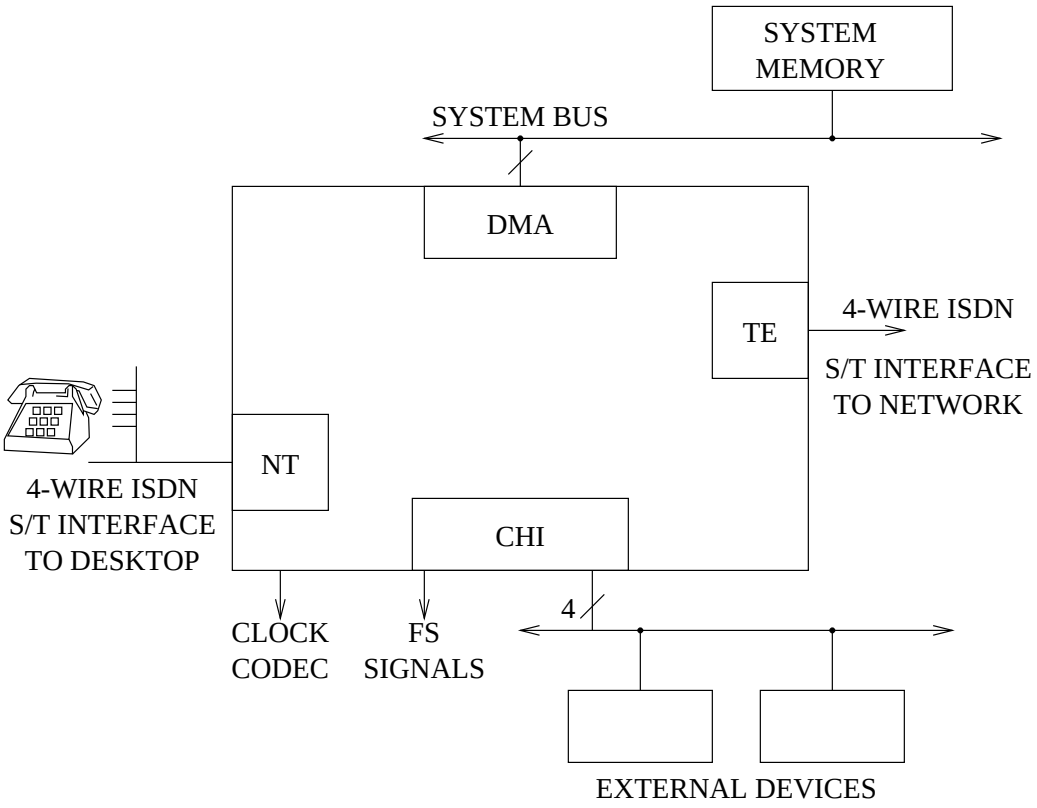

Figure 2. Application Example

Another simple application allows the DBRI to be used as a 16-channel DMA controller for external devices connected to the CHI. Examples of external devices which can be connected to the DBRI via the CHI are voice codecs, high-fidelity codecs, and video codecs. When the ISDN TE function is active, the DBRI supports the transmission of voice, data, or video over the BRI line into the network.

In the case of video conferencing, the DBRI can accept 112 kbits/s of video on one time slot of the CHI and 16 kbits/s of compressed audio on another time slot of the CHI and send 128 kbits/s of merged voice and video over the ISDN. 112 kbits/s video and 16 kbits/s audio is just an example. Any other bit rate combination of video, voice, or data can be concatenated and transmitted through the TE

interface.

The DBRI is controlled through sequences of instructions stored in system memory. In addition, there are several internal registers which are programmed by the host. The DBRI reports status and interrupts in data structures located in system memory.

Physical Interfaces

Serial Interfaces

The DBRI views the TE, NT, and CHI interfaces as independent serial interfaces.

Time Slots

A time slot is a variable length bit string derived from any of the three serial interfaces (TE, NT, or CHI). A time slot on a basic rate interface can be from 1 bit to 16 bits long; a time slot on the CHI can be from 1 bit to 255 bits long. Within the DBRI, time slots are shuttled about using a series of 32 internal pipes. There are 16 short, or shallow buffered, data pipes which are used for connection between serial ports. There are 16 long, or deeply buffered, data pipes which are used to interface between a serial port and the DMA interface to system memory.

Multiple time slots from the same interface can connect to the same data pipe, in the same direction. These time slots may or may not be contiguous (for noncontiguous mode, see DTS (0x7): Define Time-Slot Command section).

Data pipes are usually used in pairs - one in each direction. This means that any bidirectional data transfer between any of the interfaces (TE, NT, CHI, or DMA) requires two data pipes: one into the chip and one out of the chip. Each data pipe has two time slot descriptors associated with it, one for each termination point.

The ISDN S and Q channels are supported on the basic rate interfaces by the use of short data pipes. Command can be used to set a value for S and Q which is output repeatedly until changed. If an incoming S or Q channel changes, the change is reported on the interrupt queue, if this interrupt is enabled.

DMA

The DBRI has an on-chip 16-channel DMA memory address generator and buffer manager. Each DMA channel is deeply buffered with 80 bytes of FIFO.

Figure 3 highlights the use of short and long data pipes. In this application (an ISDN voice call), the CHI is not used. This application uses two short data pipes (connecting NT to TE) and four long data pipes. This application is described in detail in the Application Examples section (located in Appendix A).

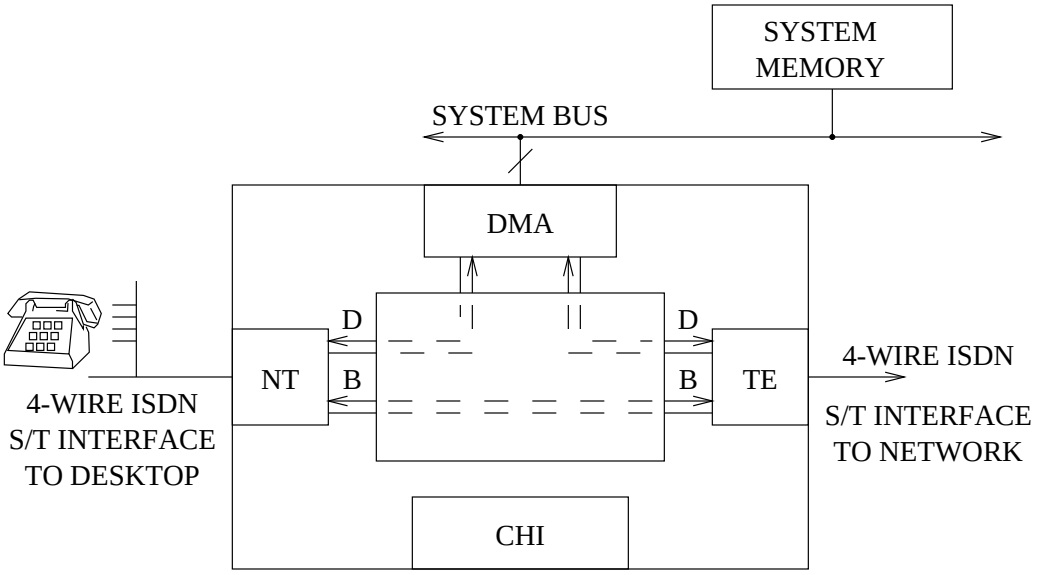

Figure 3. Short and Long Data Pipes

ISDN Interfaces

TE Interface

The TE interface enables systems to meet all CCITT Recommendation I.430 specifications for a TE at the S/T reference point when configured as shown in Figure 4. All timing is extracted from the bit and frame timing information received from the ISDN.

NT Interface

The NT interface meets all CCITT Recommendation I.430 specifications for an NT at the S/T reference point when configured as shown in Figure 4. Timing for the NT is extracted as follows. If the TE is synchronized prior to the NT becoming active, the NT frame timing is synchronous with the TE. If the TE is not active prior to the NT becoming active; then the NT frame timing is free-running. If the TE becomes active after the NT is already active, then the NT is frequency-locked to the TE but not phase-locked.

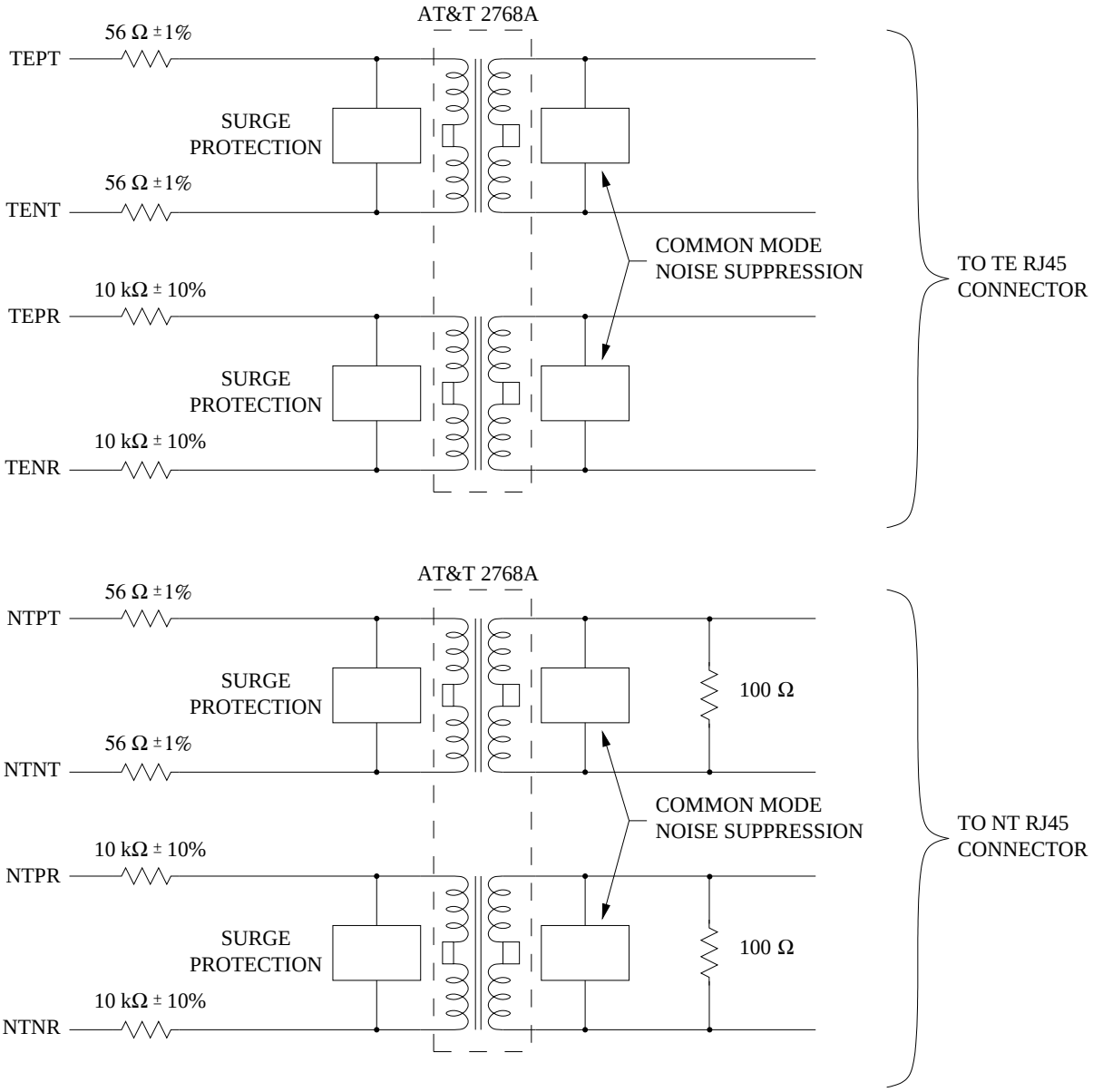

Figure 4. NT/TE Interfaces

Protection Circuitry Considerations

The AT&T 2768A dual 2.5:1 turns ratio transformer works with both the DBRI TE and NT analog front ends. The transformer is a low-capacitance design which enables the system to conform to the I.430 TE and NT impedance templates. Design of protection and noise suppression circuitry is simplified because of the margins to these templates.

The actual requirements for these circuits are highly environment (country and system) dependent. For example, the requirements for common mode noise suppression circuitry depend on system parameters such as signal rise/fall times and clock frequencies as well as the specific emissions limits used by various testing agencies (FCC class A or B, VDE, etc.). Generally, a common-mode choke is used to limit emissions out onto the line.

Surge protection circuitry is dependent upon over-voltage requirements of the testing agency. A diode bridge is usually used to shunt excessive voltage levels to ground. It should be noted that any parasitic capacitance on the device side of the transformer is increased by a factor of 6.25 (2.5 squared) when reflected to the line side. Therefore, protection circuitry capacitance may impact margin to I.430 impedance specifications.

Transformer breakdown voltage requirements also vary between regulatory agencies. The AT&T 2768A Transformer is designed to withstand 2400 Vrms for 2 s.

Concentration Highway Interface (CHI)

The CHI is a full-duplex serial time-division multiplexed (TDM) interface for digital data transfer between ICs in communication systems. The CHI can be programmed to interface with a variety of other TDM interfaces supported by various commercial products.

The CHI uses four wires: CHICK, a common data transport clock; CHIFS, a frame synchronization pulse; CHIDX, a data transmit wire; and CHIDR, a data receive wire. The clock, CHICK, can be run between 64 kHz and 6.144 MHz. The frame synchronization signal, CHIFS, can range from 8 kHz to 50 kHz when CHIFS and CHICK are inputs (CHI slave mode).

> **Important: When data is being transferred between the CHI and one of the basic rate interfaces, the CHIFS frequency must be 8 kHz.**

When an 8 kHz CHIFS is used, the CHI is viewed as a 125 µs pulse train on CHICK. When CHIFS is a non-8 kHz input, the pulse train repetition rate is set by CHIFS (see the CHI (0x9): Set CHI Global Mode Command section of this document).

The DBRI can operate as either a CHI slave or CHI master. In CHI master mode, CHIFS and CHICK are outputs; CHIFS frequency is always 8 kHz and is synchronized to the TE interface (if the TE is active). In CHI slave mode, CHICK and CHIFS are inputs to the DBRI. In this mode, CHIFS frequency can range from 8 kHz to 50 kHz.

These and other CHI options are controlled by using the Set CHI Global Mode command and by the use of the CHI anchor mode coding time-slot descriptor in a Define Time-Slot command described in the DTS (0x7): Define Time-Slot Command section of this document.

Figures 5 through 8 show the flexibility of CHI options. The CHI transmitter and receiver are programmed independently and can send/sample data on either a rising or falling edge of the clock. Data can be transmitted on any clock edge following recognition of the frame sync pulse (the number of clock edges between frame sync pulses being defined by the rate of CHICK). The frame strobe signal can be sampled on either a rising or a falling edge of CHICK.

Figures 5 through 8 show how clock edges are counted in cycles. Cycles are defined as always beginning on a rising edge, and the begin relative to the clock edge on which CHIFS is sampled.

Figure 5 shows an example of transmit timing where CHIFS is sampled on the rising edge of CHICK. If transmitting on a rising edge, then edge 2 (or the beginning of cycle 1) marks the beginning of the frame. If transmitting on a falling edge, then edge 3 represents the first transmitted bit of the frame. If transmission on edges 0 or 1 is desired, then cycle n (where n = # of bit times per frame, dependent on CHICK speed) must be used. Data transmission can begin on any clock edge relative to edge 0 by programming the appropriate CYCLE value in the Define Time-Slot command, described in the DTS (0x7): Define Time-Slot Command section of this document.

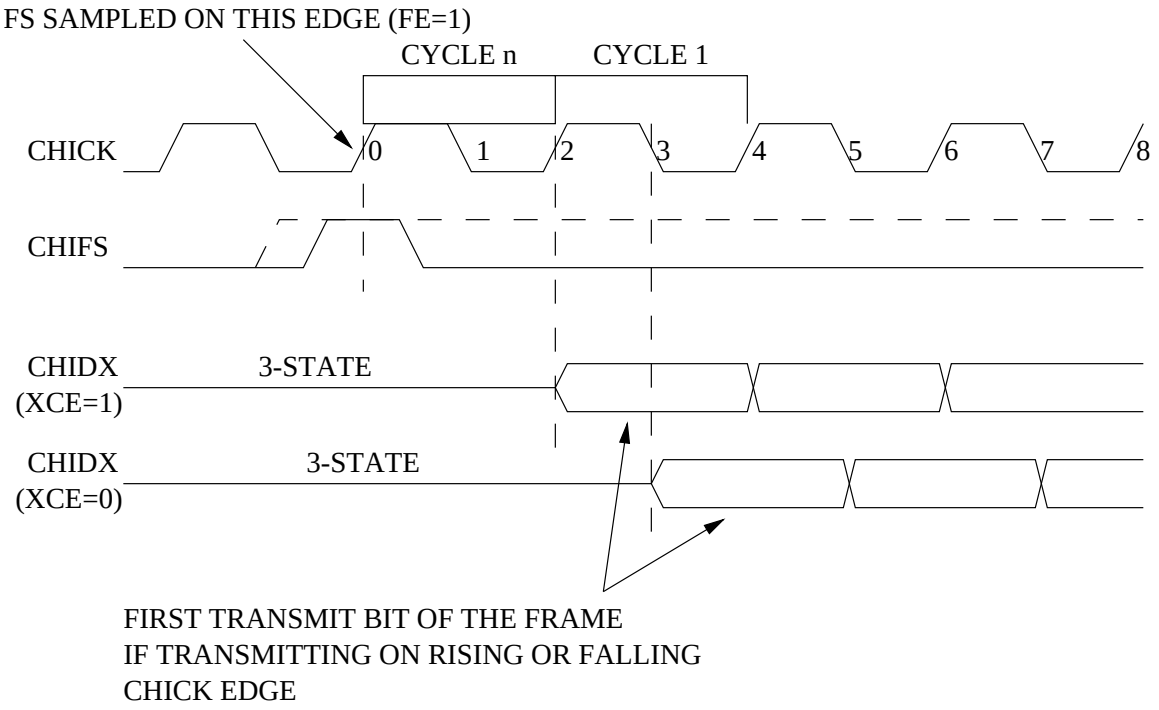

Figure 5. Transmit Timing (FE=1)

Figure 6 shows the timing when CHIFS is sampled on the falling edge of CHICK.

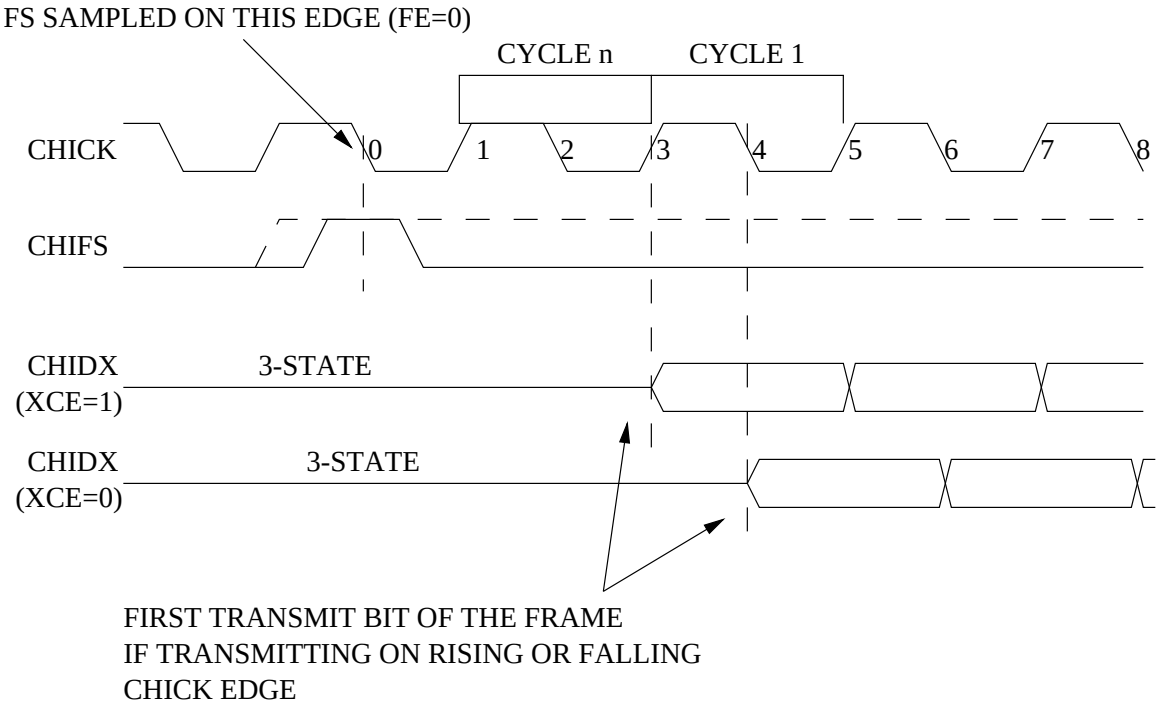

Figure 6. Transmit Timing (FE=0)

When receiving on the CHI, the location of the first bit received is programmed in the Define Time-Slot command, with one difference from the transmit case. The cycle beginning immediately after the frame strobe is sampled is called cycle 0 (instead of cycle n as in the transmit case). This is

shown in Figures 7 and 8.

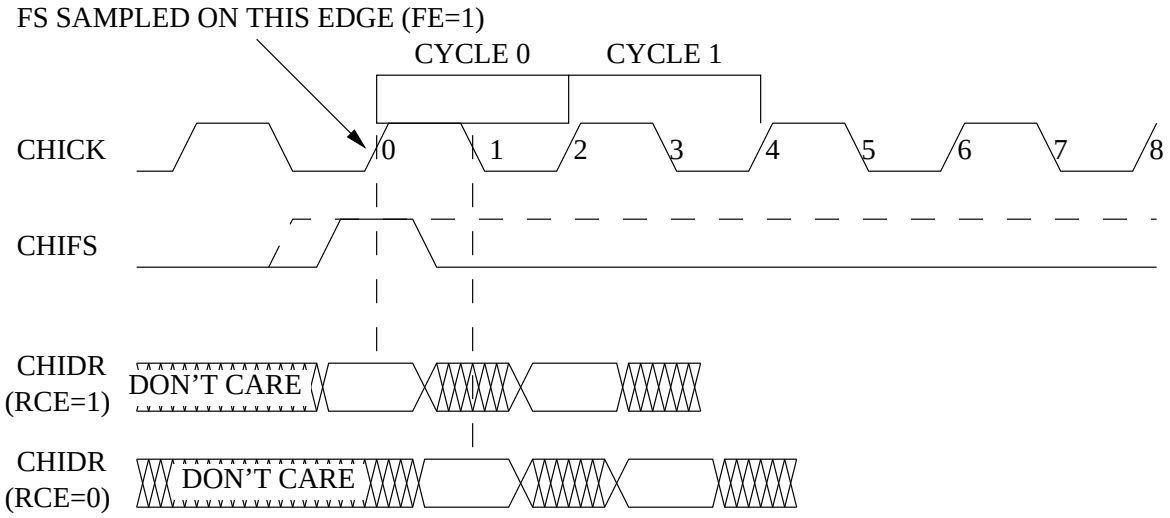

Figure 7. Receive Timing (FE=1)

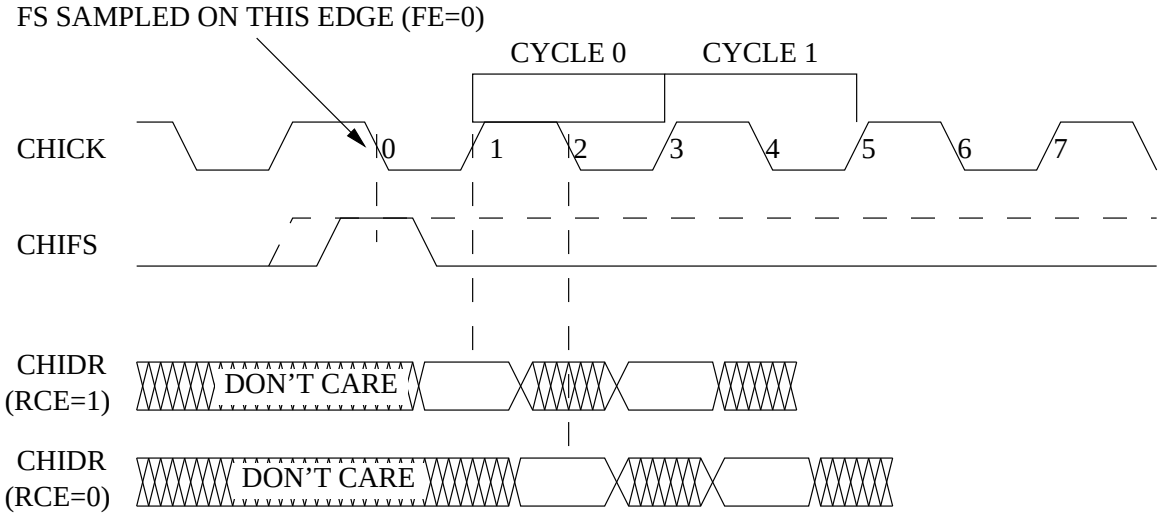

Figure 8. Receive Timing (FE=0)

The CHI can divided into logical time slots of variable length (from 1 to n bits where n is dependent on the rate of CHICK). Several devices can be connected to the CHI, each with its own transmit and receive time slot(s) assigned. In a video conferencing example, the DBRI can be connected via the CHI to a video compression chip and an audio chip. The DBRI can read 14 bits of video from one time slot and 2 bits of audio from another time slot. The DBRI can then be programmed to concatenate that data onto two B channels and send it out over the TE interface toward the network. The location and duration of a time slot on the CHI are programmed using the Define Time-Slot command described in the Commands section of this document.

Note: Avoid defining time slots which wrap around a frame boundary.

Codec Clock and Frame Sync

Data transfer between the DBRI and a codec (audio or video) occurs through the CHI. Since more than one device could be connected to the DBRI on the CHI, the CHI clock and/or frame sync might not be appropriate for the codec being used.

The CKCOD output is provided to allow the codec to operate regardless of the CHI clock frequency. FSCOD is provided to allow a nonprogrammable codec to transmit and receive data in any CHI time slot. CKCOD and FSCOD are both generated from the rising edge of the DBRI internal 12.288 MHz digital phase-locked loop (DPLL) clock, so they are synchronous with each other and phase-locked with the CHI. CKCOD and FSCOD can be used only when the DBRI is the CHI master; otherwise, they are disabled (held high).

CKCOD is a 1.536 MHz or 2.048 MHz clock derived by counting the DPLL. Most voice-based codecs can use one of these two frequencies for their master clock. CKCOD can be disabled (held high) when it is not needed.

FSCOD is a signal whose rising and falling edges are individually programmed to occur a given number of DPLL cycles after the start of a CHI frame. This allows FSCOD to look like either an active-high or active-low pulse, with a duration of any number of DPLL clock cycles, positioned at any DPLL clock cycle boundary with the CHI frame. FSCOD can be disabled (held high) when not needed by programming the rising and falling edges to occur at the same time.

The operation of these pins is controlled by using the Codec Setup (CDEC) command.

Crystal Oscillator

A 12.296 MHz crystal can be connected between the RCLK and XTALO pins. If no crystal is used, a 12.296 MHz signal must be provided to the RCLK pin. An internal 12.288 MHz (average) signal is produced from the 12.296 MHz signal by sometimes doubling a period. The 12.288 MHz signal is used to produce the CHI clock (CHICK) as well as the ISDN basic rate timing. Because synchronization with the network is achieved by doubling a period and never dropping a period, the CHI clock never has a very short period.

JTAG Test Access Port

The test access port is a four-wire interface that complies with the IEEE P1149.1-1990 standard. This standard provides a means of selecting a value to drive each digital output and sensing each digital input through a serial interface. This procedure can be used for testing connections to and on the printed-circuit board.

Internal Data Routing

Data Pipes

The DBRI has 32 data pipes. All data transfers take place through these data pipes. Sixteen long data pipes have a DMA channel which can connect it to linked list data buffers in system memory. These data pipes can be used for DMA with optional HDLC formatting in either direction. They are called long pipes because they have enough buffering to interface to DMA (80 bytes). Sixteen other short data pipes are used for data transfer between two serial interfaces (CHI, NT, and TE) and can have time slots assigned to both ends. Each short data pipe stores up to 32 bits of data.

Data Pipes Modes

Data can enter a pipe in one of three ways:

- (DMA) Data can come from a data structure in memory via DMA.
- (Serial) Data can come from a time slot on one of the serial interfaces as defined by a time-slot descriptor (TSD) associated with the data pipe. (See the DTS (0x7): Define Time-Slot Command section).
- (Fixed I/O) Fixed data can be set by the Set Short Pipe Data (SSP) command. (See the SSP (0x8): Set Short Data Pipe Command section).

Similarly, data can leave a pipe in one of three ways:

- (DMA) Data can go to a data structure in memory via DMA.
- (Serial) Data can go to a time slot on one of the serial interfaces as defined by a TSD associated with the data pipe.
- (Fixed I/O) A change in fixed data can be reported on the interrupt queue.

Any data which is DMA or fixed on one end must be serial on the other end.

Monitor Mode. In the monitor mode, serial input from one time slot can go to two pipes. (See Monitor Mode section in the DTS (0x7): Define Time-Slot Command section).

Noncontiguous Mode. In the noncontiguous mode, multiple time slots from a serial interface can be assigned to the same pipe (see the Noncontiguous Mode section in the DTS (0x7): Define Time-Slot Command section of this document).

Time Slots

Each of the DBRI's three serial interfaces (CHI, NT, TE) can have time slots defined for them. A time-slot descriptor (TSD) must be assigned to one end of the data pipe in order for data to enter or leave that end of the data pipe via a serial interface (see the DTS (0x7): Define Time-Slot Command section).

BRI

Each basic rate interface (BRI) is viewed as a 19-bit long bit string consisting of the B1 and B2 channels (8 bits each), followed by an S or Q channel bit, and then 2 bits of D channel. A time slot on a basic rate interface can be from 1 bit to 16 bits long. B1 and B2 can be concatenated and viewed as a single 16-bit time slot. For the BRI B channels, different time-slot descriptors can be used for overlapping transmit and receive time slots.

Multiple time slots from the same interface can connect to the same data pipe in the same direction (noncontiguous mode). The time slots do not have to be contiguous. (See a description of this in the DTS (0x7): Define Time-Slot Command section).

CHI

A time slot on the CHI can be up to 255 bits long.

When an 8 kHz CHIFS is used, the CHI is viewed as a 125 µs pulse train on CHICK. When CHIFS is a non-8 kHz input, the pulse train repetition rate is set by CHIFS (see the CHI (0x9): Set CHI Global Mode Command section).

Restrictions on Time Slots

- Time slots from different interfaces cannot be connected to the same data pipe in the same direction.
- For the CHI, the time-slot descriptors must not define overlapping time slots.
- CHI time slots that are greater than 32 bits long must connect to long data pipes.
- No CHI time slot can start within 0.975 µs after the start of the previous time slot.

  The DBRI does not enforce these restrictions, but peculiar actions result from their violation.

Linked Lists

The time-slot descriptors form six circular linked lists, one in each direction for the CHI and the two BRI interfaces. These linked lists must be maintained when using the DTS command. When using any serial interface, the first time slot defined is assigned to the anchor pipe. The anchor pipes for each of the serial interfaces are described below.

The TE receive time-slot list starts with the D channel in pipe 0.

The TE transmit time-slot list starts with the D channel in pipe 1 (HDLC D mode in SDP command).

The NT receive time-slot list starts with the D channel in pipe 3.

The NT transmit time-slot list starts with the D channel in pipe 2.

Both CHI time-slot linked lists (transmit and receive) start in pipe 16 (CHI anchor pipe). When initializing pipe 16, the CHI anchor mode must be used in the time-slot descriptor (TSD) field of the DTS command. (See the Commands section of this document for a more complete description of the DTS command, and see the Application Examples section for example command sequences).

Fixed I/O Channels

ISDN S and Q channels are supported on the basic rate interface. They can be connected to short data pipes, the other ends of which are in fixed I/O mode. Commands set a value for S and Q which is output repeatedly until changed. If an incoming S or Q channel changes, the change is reported on the interrupt queue. Note that when receiving fixed data, the FXDT interrupt reports only the least significant 20 bits (see the Interrupts section of this document).

Device Configuration

DBRI Clocks

Table 6. DBRI Clocks

Clock	Frequency	Source
System Clock (SCLK)	16.67 MHz to 25 MHz	External Input
Reference (RCLK)	12.296 MHz	Crystal or External Input
DPLL (internal)	12.288 MHz	Jump Reference: Sync TE, CHI, or Free
TECK	4 kHz	DPLL Sync TE
CHICK (output)	DPLL/N	Count DPLL
CHICK (input)	64 kHz to 6.144 MHz	External Input
CHIFS	8 kHz	Count DPLL or External Input
CHIFS (input only)	8 kHz to 50 kHz	External Input
TE R (internal)	192 kHz	Count DPLL
NT R (internal)	192 kHz	Count DPLL

Frame Synchronization

The DBRI TE interface always synchronizes to its receive signal (from the network). The CHI can be either a slave or a master. If the CHI is master, it generates CHICK and CHIFS, and synchronizes these to the TE interface, if active. In CHI slave mode, the CHI synchronizes to the CHIFS input. If the TE interface is also active, data transmission between the CHI and the network can be unreliable (see the Recommendation note below).

If the TE interface is synchronized with the network before the NT interface or the CHI is active, then the NT or CHI is frequency-locked with the TE when it is activated.

If the TE interface is not active before NT or CHI (master mode), then the first one to activate (NT or CHI) is free-running. Then, the next to activate (NT or CHI) synchronizes to the first. If the TE interface then becomes active, the NT and CHI are frequency-locked to the TE interface, but are not phase-locked.

Recommendation: For data transfers between TE and either CHI or NT, activate the TE first. In this way, all interfaces are synchronized to the TE and, thus, the network.

Certain applications require a low jitter clock for the CHI. The TECK output provides a synchronized 4 kHz clock for an external analog phase-locked loop to generate a low jitter clock.

The 12.296 MHz free-running crystal oscillator is counted down to 192 kHz with an occasional extra 12.296 MHz cycle added to the 192 kHz cycle. This allows the DBRI to meet the I.430 requirements for phase jitter, both for TE and NT. This method is used to phase-lock the basic rate bit clocks.

Internal Registers

DBRI Initialization

The DBRI is initialized by writing to internal registers. On-chip registers are read and written in slave mode. When registers are read, the DBRI may force the system bus to wait one or two extra clock cycles. When REG8 is written, a new command stream is executed.

REG0 is a status and control register.
REG1 is a register that provides modes of bus support and interrupt acknowledgments.
REG2 is a 4-bit parallel input/output register.
REG3 is an 8-bit test register.
REG8 is the active program counter.
REG9 is the interrupt queue pointer.

Reserved register bits should be programmed to 0.

Physical Address

REG0, REG1, REG2, and REG3 are at physical address 0x40, 0x44, 0x48, and 0x4C respectively. REG8 (command queue pointer) and REG9 (interrupt queue pointer) are at 0x60 and 0x64 respectively. The ID code registers are at physical address 0x00 through 0x3F and are read only.

The FCode provided by Sun Microsystems, Inc. for this version of silicon is a follows: (hex)

```
fd 00 09 ea 00 00 00 30 12 0a 53 55 4e
57 2c 44 42 52 49 65 01 14 12 04 6e 61
6d 65 01 10 01 02 a5 a6 7d 1e 01 03 a6
80 01 16 a8 63 a5 01 17 00
```

REG0: Status and Control Register

Table 7. REG0: Status Control Register Description

31-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	P	G	S	E	Reserved				X	T	N	C	F	D	H	R

Field	Bit	Name/Description
P	15	**Program Command Queue Pointer Valid.** This bit is set by the host CPU. It is also set by the DBRI when REG8 (command pointer) is written. It is cleared by the DBRI when a WAIT command is encountered on the command list. When the bit is set, the DBRI begins executing commands from system memory, starting at the location pointed to by the value in REG8.
G	14	**Allow 4-Word SBus Burst.** This bit is set by the host CPU allowing the SBus interface unit to do 4-word burst transfers. This bit is cleared when a 4-word burst fails on the SBus. This bit is set upon hardware or software reset. See SBus Operation section of this document.
S	13	**Allow 16-Word SBus Burst.** This bit is set by the host CPU allowing the SBus interface unit to do 16-word burst transfers. This bit is cleared when a 16-word burst fails on the SBus. This but is cleared upon hardware or software reset. See SBus Operation section of this document.
E	12	**Allow 8-Word SBus Burst.** This bit is set by the host CPU allowing the SBus interface unit to do 8-word burst transfers. This bit is cleared when an 8-word burst fails on the SBus. This but is cleared upon hardware or software reset. See SBus Operation section of this document.
X	7	**Sanity Timer Disable.** This bit is set and cleared by the host CPU. If this bit is set, the sanity timer is reset and disabled (TO pin held high). Clearing this bit restarts the sanity timer.
T	6	**Permit Activation of the TE Interface.** This bit is set and cleared by the host CPU.
N	5	**Permit Activation of the NT Interface.** This bit is set and cleared by the host CPU.
C	4	**Permit Activation of the CHI Interface.** This bit is set and cleared by the host CPU.
F	3	**Force Sanity Timer Time-Out.** This bit is set and cleared by the host CPU. Setting this bit forces an immediate time-out of the sanity timer (overrides X bit). With the F bit set, the TO pin is low and remains low until this bit is cleared. This bit is set upon both hardware and software reset. Unless the F bit is cleared, the sanity timer remains in the time-out state (TO remains low) even when registers are accessed.
D	2	**Disable Master Mode.** This bit is set and cleared by the host CPU. Setting this bit immediately disables any activity initiated by the DBRI. Since DMA is disabled, the DBRI stalls, and if left set long enough, the DBRI could have overrun and underrun conditions.

Field	Bit	Name/Description
H	1	**Halt for Analysis.** This bit (H bit) is set and cleared by the host CPU. Setting the bit halts all DMA associated with the long data pipes (can be delayed) but enables the DBRI to continue execution of commands from the command queue. Any command which controls a data pipe (SDP and DTS commands) is delayed in its execution until the H bit is cleared. Issuing these commands with the H bit set is not recommended since overrun and underruns may occur.
R	0	**Soft Reset.** This bit is set by the host CPU to RESET the DBRI. This software reset generates a short internal reset signal which is active for two clock cycles. This bit is cleared internally when the ID code is available approximately 64 clock cycles after the software reset. This bit is also set by the hardware reset and cleared internally approximately 64 system clock cycles after the rising edge of the hardware reset. Setting this bit initiates an internal initialization procedure that releases all time slots, clears all pipes, and clears REG0 (except the R bit and F bit), REG1, REG2, and REG3. Note that the on-chip internal initialization process is completed in less than 512 clock cycles after the reset (both hardware and software), but the ID code is available in less than 64 clock cycles. Slave mode access to DBRI is inhibited until ID code is available.

REG1: Mode and Interrupt Register

Table 8. REG1: Mode and Interrupt Register Description

31-9	8	7	6	5	4	3	2	1	0
Reserved	BO	Reserved			MRR	MLE	LBG	MBE	IR

Field	Bit	Name/Description
BO	8	**Byte Order.** 1 = little endian, 0 = big endian.
MRR	4	**Multiple Error Ack on SBus.** Read only - cleared when read.
MLE	3	**Multiple Late Error on SBus.** Read only - cleared when read.
LBG	2	**Lost Bus Grant on SBus.** Read only - cleared when read.
MBE	1	**Burst Error on SBus.** Read only - cleared when read.
IR	0	**Interrupt Indicator.** Indicator that an interrupt has occurred. Read only - cleared when read.

When an interrupt occurs, one of the bits in REG1 is set and the INTR* pin is driven low. When REG1 is read, the INTR* pin is placed in a high-impedance state (deasserted), and all five interrupt bits are cleared. Byte order applies only to data in data buffers, not to descriptors or commands. RESET* zeros all bits in REG1.

REG2: Parallel I/O Register

Table 9. REG2: Parallel I/O Register Description

31-8	7	6	5	4	3	2	1	0
Reserved	ENPIO3	ENPIO2	ENPIO1	ENPIO0	PIO3	PIO2	PIO1	PIO0

Field	Bit	Name/Description
ENPIO3	7	**PIO Enable for Bit 3 (PIO3).**
ENPIO2	6	**PIO Enable for Bit 2 (PIO2).**
ENPIO1	5	**PIO Enable for Bit 1 (PIO1).**
ENPIO0	4	**PIO Enable for Bit 0 (PIO0).**
PIO3	3	**Parallel Input/Output 3.**
PIO2	2	**Parallel Input/Output 2.**
PIO1	1	**Parallel Input/Output 1.**
PIO0	0	**Parallel Input/Output 0.**

If an enable bit is set, then the PIO pin associated with that enable is driven by the associated PIO bit. If the enable bit is cleared, the PIO pin associated with that enable is in a high-impedance state. When REG2 is read, the PIO bits come from the PIO pins. This means that if signals to the PIO pins change while they are being read, the system data bus may glitch. Certain modes of the TEST command use the PIO pins for another purpose. RESET* zeros all bits in REG2.

REG3: Test Register

This register is reserved for manufacturer testing. It is normally all 0s. A reset sets the register into its normal mode. It is recommended that the user not make any use of this register.

REG8: Command Queue Pointer

Table 10. REG8: Command Queue Pointer Description

31-0
Pointer to Command Queue

When REG8 is written, the P bit in REG0 is set and the list of commands pointed to by REG8 is executed. After reset, the DBRI does not initiate any I/O until REG8 is written. REG8 can be read to see which command is being executed.

REG9: Interrupt Queue Pointer

Table 11. REG9: Interrupt Queue Pointer Description

31-0
Pointer to Interrupt Queue

Points to the top of the current interrupt queue segment. This pointer is initialized by the IIQ command.

Commands

Control of the DBRI is mostly accomplished by a string of commands in system memory. Execution of this string is started by writing REG8, the command queue pointer. Execution stops when the WAIT command is executed. Execution can be restarted by overwriting the WAIT command with an active command and setting the program active bit in REG0. Remember that arbitrarily long sequences of frames can be transmitted and received without intervening commands. (See the Application Examples section of this document for more details).

Command Set Summary

Table 12. Command Descriptions

Opcode	Command	Command Description
0x0	WAIT	Wait command.
0x1	PAUSE	Pause command.
0x2	JMP	Jump to new command queue.
0x3	IIQ	Initialize interrupt queue.
0x4	REX	Report execution of command via interrupt.
0x5	SDP	Setup data pipe.
0x6	CDP	Continue data pipe (reread NULL pointers).
0x7	DTS	Define time slot.
0x8	SSP	Set short data pipe.
0x9	CHI	Set CHI global mode.
0xa	NT	NT command.
0xb	TE	TE command.
0xc	CDEC	Codec setup command.
0xd	TEST	Test command
0xe	CDM	CHI data mode command.
0xf	Reserved	-

Each command is at least one word (32 bits) in length. The first word contains the command opcode and various status and control bits. The second word usually contains a pointer (if needed). The following list gives a brief overview of all the commands with their assigned opcodes. Bits 31-28 contain the opcode of each command. If bit 27 (I bit) is set, a CMDI interrupt is issued with the corresponding opcode in the interrupt field (for example, it can be used for diagnostic purposes to determine if a certain instruction has or has not been executed). Reserved bits should be programmed to 0.

WAIT (0x0): Wait Command

Table 13. WAIT (0x0): Wait Command Description

31	30	29	28	27	26-16	15-0
0	0	0	0	I	Reserved	Value

The WAIT command indicates that the end of the command stream has been reached. Execution of this command clears the P bit in REG0. The value is reported in b[15-0] of the interrupt field. The command queue can be extended by overwriting the WAIT command and setting the P bit in REG0 or writing REG8 with the new command pointer.

PAUSE (0x1): Pause Command

Table 14. PAUSE (0x1): Pause Command Description

31	30	29	28	27	26-16	15-0
0	0	0	1	I	Reserved	Value

The PAUSE command pauses execution of the command queue and serves the long data pipes before resuming execution of the command queue. This pause allows the DBRI to synchronize the setting up of and enabling of an interface. There are three commands used to set up the different interfaces on the DBRI (SDP, SSP, and CHI commands). Since the SDP and SSP commands may be delayed in their internal execution, the PAUSE command should be used after a group of SDP, SSP, and CHI commands to allow the desired configuration to take effect within the DBRI. After the PAUSE command, it is recommended that all time slots be defined (DTS command) and any interfaces be enabled via the TE, NT, and CDM commands. If an interface is already enabled, the same sequence of commands should be used to set up and then define a new time slot.

Simply put, the idea is to use commands to set up all parameters, modes, I/O buffers, and clocking schemes followed by a PAUSE command before the time slots are defined and the interfaces are enabled.

JMP (0x2): Jump Command

Table 15. JMP (0x2): Jump Command Description

31	30	29	28	27	26-0
0	0	1	0	I	Reserved
Pointer to New Command					

Reads pointer to new command and starts executing commands.

IIQ (0x3): Initialize Interrupt Queue Command

Table 16. IIQ (0x3): Initialize Interrupt Queue Command Description

31	30	29	28	27	26-16	15-0
0	0	1	1	I	Reserved	Value
Pointer to New Interrupt Queue						

Sets up new interrupt queue pointer. Disables interrupts (except SBus interrupts) if the pointer is NULL.

REX (0x4): Report of Execution Command

Table 17. REX (0x4): Report of Execution Command Description

31	30	29	28	27	26-16	15-0
0	1	0	0	I	Reserved	Value

The VALUE field in b[15-0] is reported via an interrupt in b[15-0] of the interrupt field. When the I bit is cleared, this command can be used as a NOP.

SDP (0x5): Setup Data Pipe Command

Table 18. SDP (0x5): Setup Data Pipe Command Description

31	30	29	28	27	26-20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	I	Reserved	IRM				MODE			D	B	P	-	A	C	-		PIPE				
Pointer to Transmit or Receive Descriptor																									

The parameters of each data pipe used are set using this command. Execution of this command initializes a long or short pipe. The bit fields are described below.

Table 18. SDP (0x5): Setup Data Pipe Command Description

<table>
<tr><th>Field</th><th>Bit</th><th>Name/Description</th></tr>
<tr><td>IRM</td><td>19, 18</td><td>Interrupt Report and Mask Bits. See the Interrupts section of this document for more detailed descriptions of these interrupts.

The FXDT, UNDR, DBYT, RBYT, COLL, EOL, IBEG, and IEND interrupts can be enabled or masked on a pipe-by-pipe basis using the IRM field as follows:

<table>
<tr><th>Interrupt</th><th>Applicable Mode</th><th>Bit 19</th><th>Bit 18</th><th>Description</th></tr>
<tr><td>FXDT</td><td>0x6 (receive only D=0)</td><td>0</td><td>0</td><td>Disable FXDT interrupt</td></tr>
<tr><td></td><td></td><td>0</td><td>1</td><td>Report second time in a row value is received</td></tr>
<tr><td></td><td></td><td>1</td><td>0</td><td>Report any changes</td></tr>
<tr><td></td><td></td><td>1</td><td>1</td><td>Report every value received</td></tr>
<tr><td>UNDR</td><td>0x0, 0x2, 0x3 (transmit only D=1)</td><td>0</td><td>0</td><td>Disable UNDR interrupt</td></tr>
<tr><td></td><td></td><td>0</td><td>1</td><td>Enable UNDR interrupt</td></tr>
<tr><td>DBYT</td><td>0x4 (transmit only D=1)</td><td>0</td><td>x</td><td>Disable DBYT interrupt</td></tr>
<tr><td></td><td></td><td>1</td><td>x</td><td>Enable DBYT interrupt</td></tr>
<tr><td>RBYT</td><td>0x4 (receive only D=0)</td><td>0</td><td>x</td><td>Disable RBYT interrupt</td></tr>
<tr><td></td><td></td><td>1</td><td>x</td><td>Enable RBYT interrupt</td></tr>
<tr><td>COLL</td><td>0x3</td><td>0</td><td>x</td><td>Disable COLL interrupt</td></tr>
<tr><td></td><td></td><td>1</td><td>x</td><td>Enable COLL interrupt</td></tr>
</table>
</td></tr>
<tr><td></td><td>17</td><td>EOL Interrupt Enable Bit. Setting this bit to one enables the EOL interrupt for a pipe.</td></tr>
<tr><td></td><td>16</td><td>In the HDLC mode, the DBRI monitors the data stream between a closing HDLC flag and an opening flag. Any transitions between flags and idle are reported via the IBEG and IEND interrupts if enabled (bit 16 set to 1).</td></tr>
</table>

<table>
<tr><th>Field</th><th>Bit</th><th>Name/Description</th></tr>
<tr><td>MODE</td><td>15-13</td><td>Mode Bits. The mode bits control the type of data that flows through the pipe.
<table>
<tr><th>Bit 15</th><th>Bit 14</th><th>Bit 13</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Transparent to/from memory (long pipes only)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>HDLC (long pipes only)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>HDLC D channel (priority control for D channel transmit pipe to TE interface - pipe 1 only)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Serial in to serial out (no DMA long and short pipes)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Fixed data (no DMA short pipes only)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>D</td><td>12</td><td>Direction.
D=1: from DMA or fixed data to a serial interface
D=0: from a serial interface to DMA, from a serial interface for FXDT interrupt generation, or serial to serial.</td></tr>
<tr><td>B</td><td>11</td><td>Bit Order within Byte. If B is set, MSB is transmitted first; if B is cleared, LSB is transmitted first (DMA pipes only). Short pipes transmit LSB first.</td></tr>
<tr><td>P</td><td>10</td><td>Pointer (PTR). If PTR is set, the pointer points to the new TD/RD descriptor which should be used following the current frame. To halt a pipe, set the PTR bit with a NULL pointer.</td></tr>
<tr><td>A</td><td>8</td><td>Abort (ABT). This bit applies only to out-bound data. This bit is ignored for in-bound (receive) data pipes. If ABT is set, an ABORT is inserted into the data FIFO. If it happens in the middle of some frame, the frame is aborted and the ABT bit in the TD status is set. If it is placed in some interframe data (FLAGS or IDLES), it simply is transmitted (HDLC mode only, long pipes only).</td></tr>
<tr><td>C</td><td>7</td><td>Clear (CLR). Clear the pipe. Any frame or interframe data in the pipe is lost! It is recommended that a pipe be cleared whenever it is set up for the first time (long and short pipes).</td></tr>
<tr><td>PIPE</td><td>4-0</td><td>Pipe Identification Number. 0-15 for long pipes; 16-31 for short pipes.</td></tr>
</table>

CDP (0x6): Continue Data Pipe Command

Table 19. CDP (0x6): Continue Data Pipe Command Description

31	30	29	28	27	26-5	4	3	2	1	0
0	1	1	0	I	Reserved	PIPE				

The CDP command causes a DMA channel which has stopped because of a NULL pointer to reread the pointer to the next TD or RD. The CDP command should be placed on the command queue whenever the transmit or receive descriptor (TD/RD) queue for a specific pipe is extended. If the DBRI has encountered a NULL pointer (i.e., end of list), it rereads the pointer and continues. If the DBRI has not encountered the NULL pointer, it ignores the CDP command and continues processing the TD/RD lists with no interruption. CDP is only valid for data pipes 0-15.

DTS (0x7): Define Time-Slot Command

Any data pipe connecting to any of the serial interfaces (CHI, TE, or NT) must have a time slot assigned to it, defined by this command.

Table 20. DTS (0x7): Define Time-Slot Command Description

31	30	29	28	27	26-18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	I	Reserved	VI	VO	I/D	Prev. In PIPE					Prev. Out PIPE					PIPE				
Input Time-Slot Descriptor														Monitor PIPE					Next PIPE				
Output Time-Slot Descriptor														Monitor PIPE					Next PIPE				

Field	Bit	Name/Description
VI[1]	17	**Valid Input Time-Slot Descriptor.** Indicates that this DTS command is being used to describe the input to a data pipe.
VO[1]	16	**Valid Output Time-Slot Descriptor.** Indicates that this DTS command is being used to describe the output to a data pipe.
I/D	15	**Insert/Delete.** 0: Delete time slot from linked list 1: Add/Modify time slot to linked list
Prev. In PIPE	14-10	**Previous In Pipe.** Pipe preceding this pipe in the input list.
Prev. Out PIPE	9-5	**Previous Out Pipe.** Pipe preceding this pipe in the output list.
PIPE	4-0	**Pipe.** Pipe number for these descriptors.
Monitor PIPE	9-5	**Monitor Pipe Identifier.** Valid only for MODE 2 & 3 (see BRI and CHI mode descriptions below).
Next PIPE	4-0	**Next TSD/Data Pipe.**

[1] For programming simplicity, a serial-to-serial data pipe can have its input and output time slots defined by using one DTS command (both VI and VO set to one) or separately by the using of two DTS commands. Serial-to-DMA or DMA-to-serial data pipes would have only one direction defined per DTS command.

BRI Time Slots

Table 21 describes the input TSD and output TSD fields for the BRI interfaces.

Field	Bits	Description
LEN	31-24	**Length.** Number of bits in time slot.
CYCLE	23-14	**Cycle.** Bit count at start of time slot.
DI	13	**Data Invert.** DI = 1 to invert data.
-	12	**Reserved.** Program to 0.
MODE	11-10	**Mode.** 00 Single channel (normal operation). 01 Not used. 10 Monitor pipe input. The DBRI allows a new data pipe to be established which taps or monitors the input data through another pipe. 11 Noncontiguous mode (for multitime-slot channels).

The BRI interfaces are viewed as 19-bit long serial interfaces. B1, B2, D and S/Q channels have predetermined cycle and length values which must be used in the input and output TSD fields. Table 22 shows these values.

Channel	CYCLE	LEN
B1	0	8
B2	8	8
S/Q	16	1
D	17	2
B1 and B2 Channels Concatenated (128 kbits/s channel)	0	16

CHI Time Slots

Table 23 describes the input TSD and output TSD fields when using the CHI.

Table 23. CHI Anchor Mode Input/Output Time-Slot Descriptor.

Field	Bits	Description
LEN	31-24	**Length.** Number of bits in time slot.
CYCLE	23-14	**Cycle.** CHICK count at start of time slot.
DI	13	**Data Invert.**
MODE	12-10	**Mode.** 000 Single channel (normal operation). 001 Not used. 010 Monitor receive pipe (tee). 011 Noncontiguous mode. 100 Not used. 101 Not used. 110 Not used. 111 Anchor mode. This mode is used only when defining the CHI anchor pipe. In this case, LENGTH, CYCLE, and DI are ignored.

Linked List Management

Time-slot descriptors (TSD) form six circular linked lists internal to the DBRI, one in each direction for the concentration highway and the two basic rate ISDN interfaces. When a new time slot is deleted, added, or modified, the DTS command must always have a valid pointer to the preceding time slot so the linked list can be maintained.

Note: Time slots **must** be assigned in the order they occur on the BRI and CHI!

The time-slot descriptor must also always have a valid pointer to the next time-slot descriptor (or to itself if it is the only time slot defined for that serial interface). For data pipes that are not serial-to-serial only, one time-slot descriptor is used. The user must indicate which time-slot descriptors are valid by setting bit 17, the valid input time-slot descriptor bit (VI), and/or bit 16, the valid output time-slot descriptor bit (VO). Whenever a time slot is defined, it **must** be assigned to a data pipe.

The input/output TSDs are ignored when time slots are deleted although the VI/VO bits need to be set indicating if the time slot to be deleted is an outgoing (VO = 1) or incoming (VI = 1) time slot.

Anchor Pipes

Whenever the concentration highway is used, short pipe #16 (CHI anchor pipe) **must** be used to start both transmit and receive linked lists for the CHI interface and thus cannot be assigned to a time slot. The mode must be set to 7, CHI anchor mode. The first CHI TSD must use the CHI anchor mode to establish an anchor pipe from which all other time slots are linked. Whenever the basic rate interfaces

are used, the D-channel **must** be set up first with the following assignments:

The TE receive time-slot list starts with the D channel in pipe 0.

The TE transmit time-slot list starts with the D channel in pipe 1.

The NT receive time-slot list starts with the D channel in pipe 3.

The NT transmit time-slot list starts with the D channel in pipe 2.

It is not recommended that the D channel be passed directly between the TE and NT interfaces.

Monitor Mode

Monitor mode allows an incoming time slot to connect to two pipes. Monitor mode can only be assigned to an incoming time slot (receive only) and uses an additional data pipe. This pipe is defined using the monitor pipe field. No DTS command is necessary for the monitor data pipe.

Note that a monitor pipe goes away when the time slot is deleted.

Noncontiguous Mode

If multiple time slots need to be assigned to the same pipe (noncontiguous mode), the following procedure should be used to set up the data pipe and define the time slots.

Note: Time slots **must** be defined in the order that they occur in the frame.

1. Set up appropriate data pipes via SDP commands.
2. Define the first time slot as if it were the only time slot assigned to that pipe (mode = 0).
3. Define the following time slot as if it were the only time slot assigned to another pipe (this pipe is a sacrificial long or short pipe). Set the mode to noncontiguous mode (mode = 3), and place the pipe you want to associate with this time slot in the monitor pipe identifier.

Note: Attributes from the original SDP command apply to all time-slot segments.

SSP (0x8): Set Short Data Pipe Command

Table 24. SSP (0x8): Set Short Data Pipe Command Description

31	30	29	28	27	26-5	4	3	2	1	0
1	0	0	0	I	Reserved	PIPE				
Data										

When a short pipe is sending fixed data to a serial interface, the SSP command is used to set or change the data being sent. This is useful for the S channel on the TE interface and the Q channel on the NT interface. If bit 4 is not set (indicating a long pipe has been selected), the command is ignored. PIPE must be an outgoing pipe (D bit in SDP command must be set; D = 1). When fixed data is assigned an outgoing time slot, the number of bits used from the data field is the number of bits programmed in the

LEN field of the DTS command. The only two exceptions are the BRI S and Q time slots. The BRI S channel uses the least significant 20 bits. The BRI Q channel uses the least significant 5 bits.

Note: Data should be adjusted low order first.

CHI (0x9): Set CHI Global Mode Command

The control bits are defined as follows:

Table 25. CHI (0x9): Set CHI Global Mode Command Description.

31	30	29	28	27	26	25	24	23-16	15	14	13	12	11	10-0
1	0	0	1	I	-			CHICM	IRM		OD	FE	FD	BPF

Field	Bits	Description
CHICM	23-16	**CHI Clock Mode.** >=3 CHICK is an output (CHI master mode). CHICK rate is 12.288 MHz clock divided by CHICM. CHIFS is 8 kHz output. 0 CHICK is an input. CHIFS is 8 kHz. 1 CHICK is an input. CHIFS is not 8 kHz.
IRM	15	**Interrupt Report and Mask Bits.** If set, a CHIL interrupt gives an immediate report of the CHI status.
IRM	14	**Interrupt Report and Mask Bits.** If set, the CHIL interrupt is enabled.
OD	13	**Open-Drain Enable.** 0 Push-pull driver: Active pull-up on CHIDX or CHIDR. 1 Open-drain driver: No active pull-up on CHIDX or CHIDR.
FE	12	**Frame Edge.** 0 CHIFS is sampled on falling edge of CHICK. 1 CHIFS is sampled on the rising edge of CHICK.
FD	11	**Frame Drive.**Used only if CHIFS is driven (CHI master mode). 0 CHIFS is driven on the falling edge of CHICK. 1 CHIFS is driven on the rising edge of CHICK.
BPF	10-0	**Bits Per Frame.** When the CHI is in master mode (CHICM >= 3), CHICK outputs BPF+1 pulses per 125 µs frame. If BPF+1 defines fewer cycles than can actually occur in 125 µs (given the CHICK rate defined by CHICM), then CHICK outputs BPF+1 cycles and then remains low until the next frame. BPF does not force a frame to be longer than 125 µs. When the CHI is in slave mode (CHICM = 0 or 1), the BPF field is ignored.

The CHI command establishes the way the CHI clock is generated in master mode. It also defines CHIFS frame sync clocking, and certain global drive and report conditions. The BPF (bits per frame) field in the CHI command results in BPF + 1 CHICK cycles with the first cycle occuring the cycle before the frame sync.

NT (0xA): NT Command and TE (0xB): TE Command

The control bits are defined as follows.

Table 26. NT (0xA): NT Command and TE (0xB) Command Description.

31	30	29	28	27	26-0
1	0	1	0	I	Control Bits

Field	Bits	Name/Description
FBIT	17	**Frame Bit.** Accepts an F bit which is not a bipolar violation after an errored frame.
NBF	16	**Number of Bad Frames to Lose Framing.** NBF=0 requires 3 bad frames to lose framing. NBF=1 requires 2 bad frames to lose framing.
IRM	15	**Interrupt Report and Mask Bit.** If set, an immediate report of the BRI status is forced. See the SBRI (0x09) BRI Status Change INFO Interrupt section in the Interrupt Description Detail section.
IRM	14	**Interrupt Report and Mask Bit.** If set, the SBRI interrupt is enabled.
ISNT	13	**ISDN TE/NT Interface.** Either of the DBRIs two ISDN interfaces can be configured as a TE or an NT. If ISNT=1, the interface is configured as an NT. If ISNT=0, the interface is a TE.
FT	12	**Fixed Timing.** If ISNT=1 (NT) and FT=1 (fixed timing), the incoming data is sampled at a fixed delay (synchronous) from the transmitter. If ISNT=1 (NT) and FT=0, the incoming data is sampled by an adaptive timing mechanism. If ISNT=0 (TE), then FT **must** be set to 0 (FT=0), and the normal adaptive timing is used on the receiver.
EZ	11	**Echo Channel is Zeros.** If ISNT=1 (NT) and EZ=1, the E channel is all 0s. If ISNT=1 (NT) and EZ=0, the E channel echoes the received D channel. If ISNT=0 (TE), then EZ **must** be set to 0 (EZ=0).
IFA	10	**Inhibit Final Activation.** For links in point-to-point configurations, an interface is automatically activated when frame synchronization occurs. In multilink configurations, it may be necessary to be able to achieve frame synchronization without fully activating the link. Setting this bit allows this to happen.

Field	Bits	Name/Description
ACT	9	**Activate Interface.** This bit is used in conjunction with the T and N bits in REG0. If the T/N bit(s) are set, then the TE/NT interface responds to a request to activate but does not initiate activation of its interface unless ACT is set. The ACT is ignored until the T/N bit(s) are set. If the T/N bit(s) are set and ACT=1, then the TE/NT interface initiates activation.
MFE	8	**Multiframe (S and Q Channels) Enable.** If ISNT=1 (NT) and MFE=1, then S-channel transmission is enabled. If ISNT=0 (TE) and MFE=1, then Q-channel transmission is enabled. A TE must also detect multiframing before it activates Q.
RLB	7-5	**Remote Loopback for D (bit 7), B1 (bit 6), and B2 (bit 5).** See Loopbacks section on next page.
LLB	4-2	**Local Loopback for D (bit 7), B1 (bit 6), and B2 (bit 5).** See Loopbacks section on next page.
FACT	1	**Force Activation.** This bit, when set, allows local loopback and other tests of the interface without requiring framing from the other end of the line.
ABV	0	**Activate Bipolar Violation.** Additional BPVs are recognized as illegal. When 0 (strict CCITT mode), extra bipolar violations BPVs do not cause loss of frame synchronization. When set, extra BPVs are treated the same as missing BPVs for loss and recovery of frame synchronization. In either case, extra BPVs are reported in SBRI interrupts, if enabled.

Loopbacks

The TE and NT basic rate serial interfaces can be configured in several kinds of loopback modes. The programmer can configure either the D, B1, and/or B2 channel in a remote loopback (RLB) or local loopback (LLB) mode. Remote loopback mode puts data from the receiver on the transmitter with an octet delay. The data on the receiver can be buffered in a receive pipe. Local loopback mode buffers data from the transmitter into the receiver data pipe ignoring what is on the receiver.

Note: Neither LLB or RLB mode causes BRI interface to wake up.

CDEC (0xC): Codec Setup Command

The control bits are defined as follows:

Table 27. CDEC (0xC): Codec Setup Command Description

31	30	29	28	27	26	25	24	23	22-12	11	10-0
1	1	0	0	I	-	CK		-	FSCOD Falling Edge Delay	-	FSCOD Rising Edge Delay

Field	Bits	Name/Description
-	11,23,26	**Reserved.**
CK	25,24	**Clock Select.** 00 Disables CKCOD (forces it high). 01 Selects 2.048 MHz CKCOD. 10 Selects 1.536 MHz CKCOD. 11 Reserved.
FSCOD Falling Edge Delay	22-12	**FSCOD Falling Edge Delay.** The falling edge of FSCOD occurs this number of DPLL clock cycles after the start of a CHI frame.
FSCOD Rising Edge Delay	10-0	**FSCOD Rising Edge Delay.** The rising edge of FSCOD occurs this number of DPLL clock cycles after the start of a CHI frame. If the rising and falling edge delays are set to the same value, FSCOD always remains high.

Since there are only 1536 DPLL cycles in a CHI frame, a number greater than 1535 is ignored.

TEST (0xD): Test Command

This command provides a way to test features which would otherwise be hard to test.

Note that tests 0x5-0x8 are nondestructive; in other words, they do not interfere with any serial activity. Test 0x5 can be destructive if another device is driving PIO[0-3] or can be destructively programmed by PIO[0-3]. Tests 0x9-0xc are destructive. Any activity on the serial interfaces is lost or destroyed by executing these tests.

Table 28. TEST (0xD): Test Command Description

31	30	29	28	27	26	25-16	15-11	10-0
1	1	0	1	I	-	RAM Pointer	Size	Test Type
Pointer to System Memory (SRC Pointer for COPY)								
DEST Pointer (Only Used for COPY)								

Test Type	Name/Description
0x5	**ROM Monitor On/Off.** Toggles ROM opcode monitor on/off. When enabled, the four most significant bits of each instruction executed is driven on the PIO[0-3] pins of the DBRI. This command does not interfere with operation of the DBRI in any way except the PIO pins.

<table>
<tr><th>Test Type</th><th>Name/Description</th></tr>
<tr><td>0x6</td><td>µP Test/Copy. This test does initiate an µP master mode read from the source address followed by a write to the destination address provided in the command. Note that this command has two pointers, the first being the source (SRC) pointer and the second being the destination (DEST) pointer. The size field is the size of the transfer. The only valid sizes are 1) 0x0: single-word transfer, 2) 0x1: two single-word transfers, 3) 0x2: three single-word transfers, 4) 0x3: four-word burst or transfer, 5) 0x7: eight-word burst, 6) 0xf: 16-word burst. Note that the DBRI does not enforce that the burst size is aligned to addresses for this test.</td></tr>
<tr><td>0x7</td><td>Serial Controller Test. Bit fields from the SDP, CDM, TE, NT, CHI and CDEC commands are stored in the serial controller. This test reads the current values of these six stored registers within the serial controller and writes them to external memory. The 32-bit pointer to system memory in the command points to the location in memory that the results are written to. The format is as follows:

WORD 0 CDM b[31-24] bits 7-0 of CDM
b[23-16] bits 7-0 of CDM
b[15-9] bits 7-1 of CDM
b[8-0] bits 8-0 of CDM
WORD 1 CDM b[31-24] bits 7-0 of CDM
b[23-16] bits 7-0 of CDM
b[15-9] bits 7-1 of CDM
b[8-0] bits 8-0 of CDM
WORD 2 TE b[31-17] 0
b[16-0] bits 16-0 of TE
WORD 3 NT b[31-17] 0
b[16-0] bits 16-0 of NT
WORD 4 CHI b[31-28] 0
b[27-0] bits 27-0 of CHI
WORD 5 CDEC b[31-26] 0
b[25-0] bits 25-0 of CDEC</td></tr>
<tr><td>0x8</td><td>RAM Read. This command reads size+1 words of the internal RAM and writes the contents in system memory using the pointer given in the command. RAM pointer points to the starting location in the internal RAM. The RAM is 624 words by 33 bits; therefore, two 32-bit words are used to write a 33-bit RAM word. The most significant bit (33rd) is written in the least significant bit of the second word.</td></tr>
</table>

Test Type	Name/Description
0x9	**RAM Write.** This command is similar to the RAM Read except the 32-bit pointer is the source for the data and the RAM pointer is the destination. Again, size+1 words of the internal RAM are written where the 33rd bit is the LSB of the second word of memory.
0xa	**RAM BIST.** This command runs a built-in self test (BIST) of the on-chip RAM. If this test is successful, a 0xffffffff is written to the address provided in the TEST command; otherwise a 0x0 is written. BIST takes 10,400 cycles to complete.
0xb	**Microcontroller BIST.** This command runs a BIST on the microcontroller. The results are also written to the address provided in the TEST command as follows: 1) 0xffffffff, 2) 0xffffffff, 3) 0xffffffff, 4) 0x10000000, 5) 0x0fff0000, 6) 0xffffffff, 7) 0xffffffff, 8) 0xffffffff, 9) 0x0fff0fff, 10) 0xffffffff, and 11) 0x00000000. Microcontroller BIST takes less than 100 cycles to complete.
0xe	**ROM DUMP.** TBD. This test must be terminated by resetting the DBRI.

CDM (0xE): Set CHI Data Mode Command

The control bits are defined as follows. A local CHI loopback can be performed by transmitting and receiving on CHIDX (THI=0 and RHI=1).

Table 29. CDM (0xE): Set CHI Data Mode Desciption.

31	30	29	28	27	26-9	8-0
1	0	1	0	I	Reserved	Control Bits

Field	Bits	Name/Description
THI	8	**Transmit Data.** 1 Transmit data on CHIDR pin. 0 Transmit data on CHIDX pin.
RHI	7	**Receive Data.** 0 Receive data on CHIDR pin. 1 Receive data on CHIDX pin.
RCE	6	**Receive Edge.** 0 Receive on falling edge of CHICK. 1 Receive on rising edge of CHICK.
-	5,4,3	**Reserved.** Program to 0.
XCE	2	**Transmit Edge.** 0 Start transmitted data on falling edge of CHICK. 1 Start transmitted data on rising edge of CHICK.
XEN	1	**Transmit Highway Enable.** DBRI does not drive CHIDX or CHIDR when XEN is 0. Reset forces XEN to 0.
REN	0	**Receive Highway Enable.** Allows multichannel synchronization.

Interrupts

The DBRI writes an interrupt word into the interrupt queue to provide information on status and a variety of events. Each interrupt word contains the channel number, interrupt code, and interrupt field.

Table 30. Bit Assignments for Interrupt Word

Field	Bits	Description
I bits	31,30	Set by DBRI to 10 for a 32-bit interrupt. They should be cleared by the host processor after the interrupt is serviced.
Channel	29-24	The DBRI channel number on which the interrupt occurred. Channels 0 to 31 are the data pipes. Channel 32 is the TE status. Channel 34 is the NT status. Channel 36 is the CHI status. Channel 38 is the command and interrupt status (CMDI and LINT interrupts).
Interrupt Code	23-20	Identifies which interrupt caused the report. **Bits 23-20** / **Interrupt** / **Description** 0x01 / BRDY / Buffer ready for processing 0x02 / MINT / Marked interrupt in RD/TD 0x03 / IBEG / Flag-to-idle transition detected (HDLC mode only) 0x04 / IEND / Idle-to-flag transition detected (HDLC mode only) 0x05 / EOL / End of list 0x06 / CMDI / Command has been read 0x08 / XCMP / Transmission of frame complete 0x09 / SBRI / BRI status change INFO 0x0a / FXDT / Fixed data change 0x0b / COLL / Unrecoverable D-channel collision (for channels 0-15, not channel 36) 0x0c / DBYT / Dropped byte frame slip 0x0d / RBYT / Repeated byte frame slip 0x0e / LINT / Lost interrupt 0x0f / UNDR / DMA underrun
Interrupt Field	19-0	Used to report a longer piece of data such as the S-channel data.

Summary of Interrupts

Table 30 shows the bit assignments for the interrupt word. The DBRI sets the I bits to 10, writes the channel number, the interrupt code, and the interrupt field, and then generates an interrupt. Following is a description of each field in the interrupt word.

Interrupt Setup

The Initialize Interrupt Queue (IIQ) command contains a full pointer (32 bits) to the beginning of the interrupt queue. Interrupts are globally enabled by an IIQ command with a valid pointer. Interrupts are globally disabled by an IIQ command with a NULL pointer. Each interrupt queue segment consists of 64 words: the first word contains a pointer to the next interrupt queue segment, and the remaining 63 words represent interrupts. Every interrupt can also be masked by cleared the appropriate interrupt control bits associated with the command, transmit, and receive descriptors.

A recommended housekeeping procedure is for the host to write 0x00000000 for interrupt queue maintenance after it services the interrupt. When the interrupt queue is full, the DBRI reads the pointer to the next interrupt and continues recording interrupts. This gives the host flexibility in making the interrupt queue arbitrarily long (in 63 word segments). The host must always provide a valid pointer in each interrupt queue. The DBRI never reads the contents of the interrupt queue. It only reads the pointer to the next interrupt queue segment. Therefore, the host must ensure that the queue does not overflow if it is circular.

Interupt Description Detail

BRDY (0x01): Receive Buffer Ready Interrupt

This interrupt applies to receive buffer operations. It indicates that the DBRI has closed a receive buffer due to an end of frame condition (closing flag or abort, HDLC) or simply that a buffer is full (transparent mode). This interrupt is masked by clearing the B bit in the receive descriptor (see Memory Structure section of this document).

Its channel numbers are from channel 0 to channel 15; the interrupt field contains the lower 20 bits of the RD address.

MINT (0x02): Marker Interrupt

This interrupt is issued as soon as the TD/RD is read. This allows interrupts which are not frame synchronous, to facilitate list management. The MINT interrupt is maskable by clearing the MINT bit in the TD/RD.

Its channel numbers are from channel 0 to channel 15; the interrupt field contains lower 20 bits of TD/RD address.

IBEG (0x03): Flag-to-Idle Transition Detected Interrupt

The IBEG interrupt is issued when a flag-to-idle transition has been detected (HDLC mode only). It is masked by bit 16 of an SDP command. This interrupt could be used to start the T3 idle timer for LAPB.

Its channel numbers are from channel 0 to channel 15; it has no interrupt field.

IEND (0x04): Idle-to-Flag Transition Detected Interrupt

The IEND interrupt is issued when an idle-to-flag transition has been detected (HDLC mode only). Masked by bit 16 of an SDP command. This interrupt could be used to stop the T3 idle timer for LAPB.

Its channel numbers are from channel 0 to channel 15; it has no interrupt field.

EOL (0x05): End of List Interrupt

This interrupt indicates that the DBRI has encountered a NULL pointer to the next TD or RD (next descriptor address, NDA). This is equivalent to a do not enter statement. The transmitter repeats the last byte(s) and rereads the pointer upon execution of subsequent CDP and SDP commands. The EOL interrupt is maskable by bit 17 of an SDP command.

Its channel numbers are from channel 0 to channel 15; if SDP command is issued with a valid pointer and PTR=1, then the ensuing EOL interrupt has an interrupt field with the lower 20 bits of the address of the NULL pointer. If an SDP is issued with a NULL pointer and PTR=1, the ensuing interrupt has an interrupt field of 0.

CMDI (0x06): Command Read Interrupt

This interrupt indicates that the first word of a command has been read by the DBRI. It can be masked by clearing the I bit in the command. The interrupt field contains the opcode of each command in bits 19-16 and bits 15-0 of the command in bits 15-0. For the WAIT, PAUSE, and REX commands, the interrupt also indicates the command has been executed.

Its channel number is channel 38 only.

XCMP (0x08): Transmission Frame Complete Interrupt

This interrupt is issued when a frame has been transferred from on-chip RAM to the serial shift register for transmission. It can be masked by clearing the B bit in the transmit descriptor (TD). The B bit is only valid when the EOF bit is set in the corresponding TD.

Its channel numbers are from channel 0 to channel 15; it has no interrupt field.

SBRI (0x09): BRI Status Change INFO Interrupt

Table 31. Meaning Bits SBRI Interrupt Field

Name	Bit	Meaning
vta	10	Voltage Threshold Adjustment. 0 High threshold selected 1 Low threshold selected
berr	9	Detectable Bit Error.
ferr	8	Frame Sync Error.
mfm	7	Multiframe Mode.
fsc	6	Frame Sync Established.
rif4	5	Activation Bit (A bit) is 1 (if TE).
rif0	4	No Signal Received.
act	3	Activate Bit (bit 9 from NT/TE command).
tss	2-0	Interface Activation State.

A change in the TE or NT interface activation state (tss bits 2-0) may cause an SBRI interrupt. A bipolar violation error after frame synchronization is achieved may cause an SBRI interrupt. It is masked by the IRM bits in a TE or NT command. Bit 14 enables this interrupt. Bit 15 forces a report of current status without a change in status. The tss field is a subset of Tables 5 and 6 in CCITT I.430 (blue book). See pages 185-187 of blue book CCITT I.430. An exception to this, after the interface has reached state F3 transitions to tss=0, must be considered F3, and transitions from tss=0 to tss=3 should be ignored. Transitions to tss=0 may be caused by noise on the line or by the driver clearing the T bit in REG0 to force a time-out transition. Transitions from tss=0 to tss=3 occur spontaneously when the line is clear. Sometimes a forced SBRI interrupt causes a state change not to report. This is most common when a TE command has bits 15 and 9 set. Tss may change from 3 to 4 between the time when the interrupt is reported and the time when the request is cleared. An F8->F7->F8 transition is possible if the A bit in the frame is 1 (see rif4). Two consecutive bad frames are needed to report ferr.

Table 32. tss Field

tss bits b[2-0]	Number	State Represented
NT, INFO0	0	Inactive and not trying to activate interface (G1 of Table 6 of blue book).
TE, INFO0	0	Inactive and not trying to activate interface (F1 of Table 5 of blue book).
NT or TE	1	Illegal code.
TE, INFO0	2	TE has lost framing (F8 in Table 5 of blue book).
NT	2,3,4,5	Illegal code.
TE, INFO0	3	TE is not seeking activation (F3 in Table 5 of blue book).
TE, INFO1	4	Sending request for activation (F4 in Table 5 of blue book).
TE, INFO0	5	Requested activation and hasn’t achieved framing (F5 in Table 5 of blue book).
NT, INFO2	6	Sending framing (G2 in Table 6 of blue book).
TE, INFO3	6	Sending framing (F6 in Table 5 of blue book).
NT, INFO4	7	Sending data (G3 in Table 6 of blue book).
TE, INFO3	7	Sending data (F7 in Table 5 of blue book).

Its channel number is channel 32 (TE) or channel 34 (NT).

FXDT (0x0a): Fixed Data Change Interrupt

The changed data is reported into the 20-bit interrupt field. The first bit received is the low-order bit. This interrupt is masked by bits 18 and 19 of an SDP command. Bits 18 and 19 of an SDP command form a number with following meanings: 0: disable FXDT interrupt, 1: report the second time in a row a value is received, 2: report any change, 3: report every value received (change or not).

Its channel numbers are from channel 0 to channel 31, but they are usually from channel 16 to channel 31.

CHIL (0x0b): CHI Lost Frame Sync Interrupt

Bit 3 in the interrupt field means that the CHI expects external frame sync and has not detected it for 250 µs (CHICM 0). Bit 2 means that the CHI receiver could not keep up. Bits 0 (RCVR active if ONE) and 1 (XMTR active if ONE) report whether the CHI transmiter and receiver are active, but does not cause an interrupt. It is masked by bit 14 in the CHI command. Bit 15 of the CHI command forces an immediate report of the CHI status.

Its channel number is channel 36 (CHI).

COLL (0x0b): Unrecoverable Collision

This interrupt is issued when a collision of a D-channel packet results in a packet or frame fragment that cannot be retransmitted. Legal LAP-D packets cannot collide late enough to cause this interrupt. The D channel must be restarted with an SDP command with the clear pipe bit set. If a single packet is presented to the DBRI each time for TE D-channel transmission, that packet should be queued again. If multiple packets are in the pipe, the queue should be restarted after the last marked frame. This forces Level II error recovery. It is masked by bit 19 of an SDP command.

Its channel number is channel 1 or channel 2 (pipe associated with the TE D channel).

DBYT (0x0c): Dropped Byte Frame Slip Interrupt

When the BRI interfaces have one clock and the CHI has an independant clock, sometimes there is not room in a data pipe for new data. This interrupt reports that condition. It is masked by bit 19 of an SDP command.

Its channel numbers are from channel 0 to channel 31; it has no interrupt field.

RBYT (0x0d): Repeat Byte Frame Slip Interrupt

When the BRI interfaces have one clock and the CHI has an independant clock, sometimes there is no data in a pipe when it is needed. This interrupt reports that condition. It is masked by bit 19 of an SDP command.

Its channel numbers are from channel 0 to channel 31; it has no interrupt field.

LINT (0x0e): Lost Interrupt Interrupt

If reportable conditions cannot be written to memory fast enough, a lost interrupt interrupt is reported. Although this interrupt cannot be masked, it cannot occur if all other interrupts are masked off. Applies to XCMP, SBRI, FXDT, CHIL, DBYT, and RBYT interrupts.

Its channel number is channel 38; it has no interrupt field.

UNDR (0x0f): DMA Underrun Interrupt

This interrupt indicates that the DBRI could not keep up with the serial port. This interrupt is not reported if the last byte sent was a flag or an idle (HDLC mode). It is masked by bit 18 of an SDP command. In HDLC mode, an underrun causes the current frame to be aborted, and the status bit in the transmit descriptor (TD) is set indicating an underrun. All TDs up to and including the TD with EOF=1 are marked with an UNR status.

It channel numbers are from channel 0 to channel 15; it has no interrupt field.

Interrupt Masks

Every condition which the DBRI reports can be masked. Depending on the type of interrupt, the mask may be the IRM bits in the relevant command or may be interrupt bits in transmit or receive descriptors.

Memory Structure

The value loaded in REG 8 is the pointer to the command queue in external memory. All DBRI data structures are aligned on 32-bit word boundaries. Transmit descriptor and receive descriptor buffers must be aligned on 4-word boundaries.

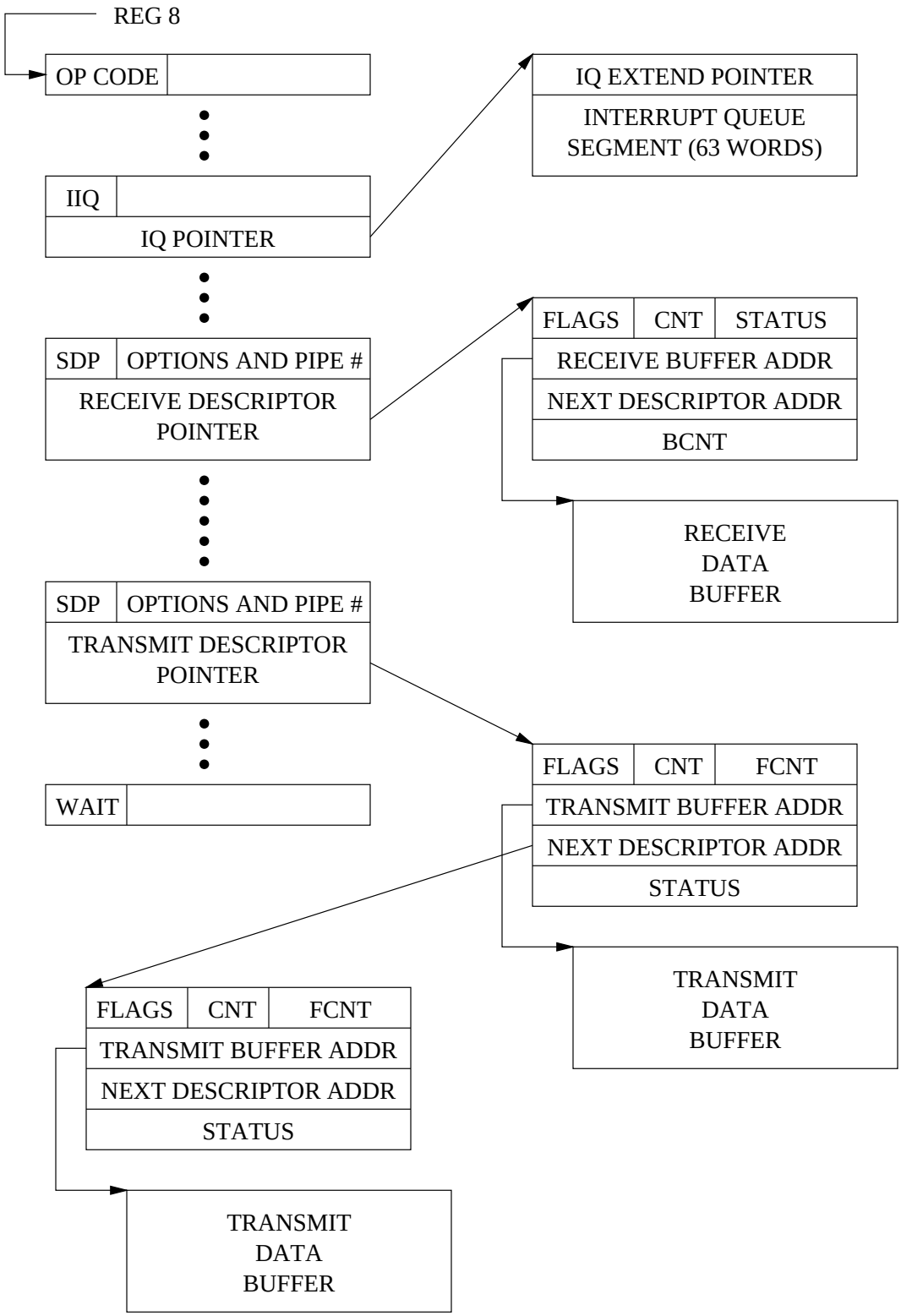

Figure 9. Memory Structure for Dual Basic Rate ISDN Interface Chip

For each transmit channel, there is a linked list of transmit descriptors (TD). Each TD has a buffer pointer and a byte count. An HDLC frame can be made of one or more TDs and buffers. For each receive channel, there is a linked list of receive descriptors (RD). Each RD has a buffer pointer and a buffer size field. An HDLC frame can require one or more RDs and buffers. When a frame is complete, the DBRI sets the actual byte count and status information. The command stream and interrupt queue have already been described.

Transmit Descriptors

The transmit descriptor (TD) contains a pointer to the next TD, a pointer to the transmit buffer (TB), the length of the transmit buffer (CNT), the fill flag count (FCNT), and the control bits. The DBRI stores CNT in on-chip memory and decrements it by one whenever a byte is transmitted.

If the EOF bit is set, the DBRI reads FCNT after transmitting CNT data bytes and sends at least FCNT+1 flags or idles (HDLC mode). Otherwise, the DBRI opens the next TD and continues to send data in a continuous frame. In this manner, data for a frame can be spread across several TDs. The DBRI then reads the next TD address (NDA) and writes the status word. The functions described above are repeated until the host issues a Setup Data Pipe (SDP) command to break the chain or the end of the list is encountered (NULL pointer). If a NULL pointer is encountered, the DBRI repeats the last FLAG/IDLE (depending on I bit in TD) for HDLC mode or repeats the last byte(s) for transparent mode.

Table 33. Transmit Descriptor

31	30	29	28-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F	D	-	CNT: Byte Count	B	M	I	FCNT: Flag Count												
Transmit Buffer Address (TBA)																			
Next Descriptor Address (NDA)																			
Reserved																Status			

Field	Bits	Name/Description
EOF(F)	31	**End of Frame.** This bit is set by the host if the frame is completed by data in the associated buffer. The DBRI appends the CRC at the end of the frame if required (i.e, the DCRC bit = 0). If CNT=0 and EOF is not set, then one flag or one idle code (16 1s) is transmitted (depends on previous TD I bit setting).
DCRC(D)	30	**Do Not Append CRC. (HDLC Only).** The CRC is not appended to the current frame if this bit is set.
CNT	28-16	**Octet Count.** CNT is the number of the data bytes in the buffer linked to a corresponding descriptor. If CNT is initially 0 and the EOF bit is set, the DBRI transmits flags or idles based on the I bit and FCNT.

Field	Bits	Name/Description
FINT(B)	15	**Final Interrupt.** The B bit is only valid when the EOF bit is set. The host sets both the EOF and B bits to have the DBRI interrupt when the end of the frame has been transferred from the internal RAM to the serial shift register for transmission. See XCMP interrupt in the Interrupt Description Detail section.
MINT(M)	14	**Marker Interrupt.** Causes an interrupt as soon as the transmit descriptor is read.
IDL(I)	13	**Transmit Idle Characters.** The host sets this bit if the DBRI is to transmit idles after the current frame. If FCNT=0, no idles are sent. Otherwise, FCNT+1 8-bit sequences of ones are sent (HDLC mode only). Valid only if EOF=1. For HDLC-D channel mode, the IDL bit and FCNT field are used to determine the number of 1s (priority class) transmitted on the TE interface D channel. These 1s are transmitted before the opening flag of the next frame. If I=0, then the opening flag is shared with the closing flag of the previous frame. This implies that the first frame after a reset or EOL condition must have IDL=1 and FCNT set to a 1 or 0 (see FCNT below). As long as the first frame has IDL=1, consecutive TDs in the TD list can have IDL=0. This means that frames are transmitted with minimal overhead (shared closing and opening flag). IDL is always valid in HDLC-D mode (independent of EOF).
FCNT	12-0	**Flag Count.** The flag count is the number of flags the DBRI inserts after the closing flag of the current frame. If FCNT=0, the closing flag is shared with the opening flag of the next frame. If the IDL bit is set, continuous 1s are sent after the closing flag of the current frame. FCNT+1 is the number of 8-bit sequences of ones that are transmitted (HDLC mode only). Valid only if EOF=1. For TE interface HDLC D channels, FCNT is read in the first TD of each frame to determine the number of 1s (priority class) transmitted before the opening flag. The number of 1s is 8 or 9 if FCNT=0 (priority class 1). The number of 1s is 10 or 11 if FCNT=1 (priority class 2). Valid in HDLC-D mode when IDL=1 (independent of EOF).
TBA	31-0	**Transmit Buffer Address.** This is the 32-bit starting address of the data buffer associated with the descriptor. Transmit buffers can begin on byte boundaries.
NDA	31-0	**Next Descriptor Address.** This is the 32-bit starting address of the next transmit descriptor on the linked list. The DBRI can be configured to interrupt the host when it encounters an NDA pointer that is NULL (see EOL interrupt in the Interrupt Description Detail section). The DBRI then sends flags or idles without regard to FCNT until it finds a good pointer after executing an SDP command or the P bit in REG0 is set. The DBRI then follows the new pointer and begins to transmit data again.

After the DBRI completes reading the data from the transmit buffer, it writes the status in the TD. All bits of the TD status words are written in the same transaction, and the TBC bit is always set when the DBRI completes use of the TD and its associated buffer. The status bits should be initialized to 0 by the host. The status bits for all descriptors are as shown in Table 34.

Table 34. Transmit Status for All Modes

7	6	5	4	3	2	1	0
Reserved				UNR	ABT	-	TBC

Field	Bits	Name/Description
UNR	3	**Underrun.** The serial transmitter ran out of data. For HDLC mode, the frame is aborted. For transparent mode, the last byte is repeated. See UNDR interrupt in the Interrupt Description Detail section.
ABT	2	**Abort.** The DBRI sets this bit if the frame is aborted while the DBRI is transmitting data bytes in the current descriptor. (HDLC mode only. See SDP command in the Commands section and UNDR interrupt in the Interrupt Description Detail section.)
TBC	0	**Transmit Buffer Complete.** The DBRI sets this bit when it has completed all accesses to the TD and its transmit buffer.

Receive Descriptors

The receive descriptor contains the size of the associated receive data buffer (BCNT), number of received bytes in the descriptor (CNT), and status of the received frame. The DBRI writes the number of received bytes in CNT when it fills the buffer (CNT = BCNT) or it receives a closing flag. The DBRI also writes the status and updates the EOF and C bits.

When the DBRI receives a frame longer than the allocated buffer, it clears the EOF bit and sets the C bit, writes the CNT, and proceeds to the next descriptor. The DBRI continues to write the received data in the buffer assigned by the new receive descriptor. The status of the received frame is written to the RD whenever an EOF condition is detected.

Table 35. Receive Descriptor

31	30	29	28-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F	C	-	CNT: Byte Count	Reserved								Status							
Receive Buffer Address (RBA)																			
Next Descriptor Address (NDA)																			
Reserved				B	M	-	BCNT: Max Buffer Length												

Field	Bits	Name/Description
EOF(F)	31	**End of Frame.** The DBRI sets the EOF bit to indicate that the current frame has ended in the buffer area for the associated descriptor. Otherwise, the frame continues in the buffer area of the next descriptor. If EOF=0 and C=1, the current frame continues in the next buffer area. EOF=1 and C=1 signifies the end of a frame and that the current buffer and entire frame are ready for host processing. The EOF bit is always set when the C bit is set in the transparent mode.
COM(C)	30	**Completed Buffer.** The DBRI sets the C bit to indicate that the buffer of the associated descriptor has been filled. This does not necessarily mean the end of the frame has been received. The DBRI **always** sets the C bit when it has completed all accesses to the RD and its receive buffer. Therefore, the host can process the buffer if this bit is set. It is the responsibility of the host to clear the first word of the RD when it is put on the receive queue for use by the DBRI.
FINT(B)	15	**Final Interrupt.** The DBRI issues an interrupt when the buffer is filled (transparent) or an HDLC frame ends in the buffer. See BRDY interrupt in the Interrupt Description Detail section.
MINT(M)	14	**Marker Interrupt.** The DBRI issues an interrupt as sson as the RD is read. This allows interrupts which are not frame synchronous for list management. See MINT interrupt in the Interrupt Description Detail section.
CNT	28-16	**Octet Count.** The count value written by the DBRI reflects the total number of data bytes stored in the data buffer associated with the current descriptor. If the EOF bit is cleared, CNT is the same as BCNT. For HDLC modes of operation, the CRC is always included in the buffer. This is reflected in the CNT field.
BCNT	12-0	**Buffer Count.** BCNT is the number of bytes the host allocates for the receive buffer. Note that BCNT must be greater than or equal to four and be a multiple of four. Frames (data delimited by an opening and closing flag) with less than three octets are not recorded, but discarded.
RBA	31-0	**Receive Buffer Address.** This is the 32-bit starting address of the data buffer associated with the descriptor. It **must** be word aligned.
NDA	31-0	**Next Descriptor Address.** The same as a transmit NDA. Note that data may be lost if a receiver runs out of buffers (see Overrun Condition Detected in Table 36).

The DBRI writes the status in the receive descriptor when it detects an EOF condition. The status field bit assignments are shown in the following table.

Table 36. Receive Status for All Modes

7	6	5	4	3	2	1	0
CRC	BBC	ABT	-	OVRN	Reserved		

Field	Bits	Name/Description
CRC	7	**CRC Status.** The CRC is correct for the received frame if this bit is cleared. Otherwise, the CRC is bad for the received frame. (HDLC; valid only when EOF=1.)
BBC	6	**Bad Byte Count.** Indicates that a partial byte has been received if set. The frame could still have good or bad CRC status. (HDLC; valid only when EOF=1.)
ABT	5	**Abort.** The ABT bit is set if the frame is aborted. (HDLC; valid only when EOF=1.)
OVRN	3	**Overrun Condition Detected.** The OVRN bit is set for an overrun condition. Data is lost from the buffer. Note that this condition cannot be reported until there are receive descriptors in the receive descriptor list. Subsequent buffers are filled normally.

Data Modes

HDLC Mode

Table 37. HDLC Frame Format

Opening Flag	Header Bytes	Information Field	CRC	Closing Flag
01111110	Up to 7 Bytes	Optional 0 to 8190 bytes	2 bytes	01111110

Note that the information field is optional. Its length ranges from 0 bytes to 8190 bytes.

The transmitter produces HDLC frame bounded by flags from the data contained in one or more transmit buffers. The CCITT 16-bit CRC is gernerated by the DBRI and appended to the user-supplied data. The polynomial used in calculating the CRC is $X^{16}+X^{12}+X^{5}+1$. The zero bit stuffing for data transparency is performed on the data between the last bit of the opening flag and the first bit of the closing flag.

The receiver recognizes the start of a frame by searching the incoming data stream for a nonflag octet following a flag. It then removes the zeros that were inserted for data transparency, writes this data into one or more receive buffers, and performs the CRC detection checks until a closing flag is detected.

Zero Bit Insertion/Deletion (Bit Stuffing/Unstuffing)

The DBRI performs the bit stuffing and unstuffing for the information field on the data set up in the TDs to maintain data transparency. A zero bit is inserted (bit stuffing) into the transmitted bit stream after five ones. The receiver deletes a zero immediately following five ones. The purpose of bit stuffing all data internal to the frame is to permit the use of a flag character (01111110) to delineate a frame and abort (01111111) and idle (11111111) characters. Whenever the receiver encounters more than five consecutive 1s, it is interpreted as part of one of these special characters.

Flag

The flag has the binary representation of 01111110 (7E hex) and is used for frame delineation. The flags are also used as fill characters between frames. If the receive unit receives one flag between two frames, the DBRI recognizes it has the closing flag of one frame and also the opening flag of the next frame. The transmit unit always transmits at least one flag between successive frames, and an additional number of flags may be transmitted by programming the FCNT field in the transmit descriptor. This is described in detail in the Memory Structure section.

The receive unit also recognizes two or more successive flags which share the zero bit in between them (011111101111110). The transmit unit does not share the zero bit between flags (i.e, 0111111001111110 is transmitted).

Short Frames

Frames less than 24 bits long, including CRC, are dropped and not reported. No common protocols use frames less than 32 bits including CRC.

Abort

The abort character has the binary representation of 01111111 (7F hex). The transmit unit sends the abort if the ABT bit in the SDP command is set. The receiver interprets seven consecutive 1s as an abort.

Idle

The idle character has the binary representation of 11111111 (FF hex). A number of idle characters equal to FCNT can be transmitted between frames as an alternative to the flags. The opening and closing flag are still sent to delimit the frame. When receiving data, an idle condition is detected after receiving 15 consecutive ones.

Transparent Mode

In the transparent mode, the DBRI transmits the data without any bit manipulation. For the receive channels, the DBRI continues to write the received data into system memory as specified in the receive descriptor. The receiver continues to fill the buffers until a NULL pointer is encountered or the host (via a command) stops the receiver from buffering data.

JTAG Specification

Instruction Register

The instruction register (IR) is 3 bits in length (minimum length with no parity bit). The instructions are defined as follows:

Table 38. Instruction Register Description

Instruction	Hex	Binary (type)
EXTEST	0	000 (mandatory)
IDCODE	1	001 (optional)
SAMPLE/PRELOAD	2	010 (mandatory)
HIZ	3	011 (design-specific)
BYPASS	4	100 (mandatory)
BYPASS	5	101 (mandatory)
BYPASS	6	110 (mandatory)
BYPASS	7	111 (mandatory) LSB shifted in JTDI first

The following instructions are optional and are not supported in this device: INTEST, RUNBIST and USERCODE. A fixed binary 001 pattern (the 1 in the LSB) is loaded into the IR in the capture IR controller state. The IDCODE instruction (binary 001) is loaded into the IR during the test-logic-reset controller state and also at powerup.

The following is an explanation of each instruction and its effect on the device pins.

EXTEST

This instruction places the boundary-scan resister (BSR) in the scan chain. EXTEST forces the outputs and enables for any 3-statable or bidirectional pins to the value in the holding resister. The holding register can be preloaded using the SAMPLE/PRELOAD instruction prior to the EXTEST instruction. Otherwise, the state of the outputs and bidirection pins is unknown.

IDCODE

This instruction places the device identification register in the scan chain. Manufacturer’s ID for Sun Microsystems, Inc. is 0x3E. The device ID register value for the current silicon is 0x50BD107D.

SAMPLE/PRELOAD

This instruction places the BSR in the scan chain. SAMPLE/PRELOAD samples the state of the pins and enables. The sampled values are shifted out, and another pattern is shifted in on JTDI (PRELOAD). The new values are not forced on the pins, but are held in the holding register.

HIZ

This instruction places the BYPASS register in the scan chain. It also forces all 3-statable outputs to a high-impedance state and all bidirectionals to an input state.

RD, SIZ[2-0], ACK[2-0]*, D[31-0] are all inputs.
PIO[3-0] are inputs.
CHICK, CHIFS, CHIDX, and CHI are inputs.
TECK, CKCOD, FSCOD, TO, and INTR are 3-stated.

BYPASS

This instruction places the BYPASS register in the scan chain.

Boundary-Scan Register

The boundary-scan register (BSR) is 88 bits in length. The following are descriptions of each cell in the boundary-scan chain beginning at the LSB. No cell can apply its value to on-chip logic.

Table 39. Boundary-Scan Register

Name	BS Reg Bit #	Description
PIO[0-3]	0-3	Bidirectional.
EN_PIO0	4	PIO0 input when EN_PIO0 = 0.
EN_PIO1	5	PIO1 input when EN_PIO1 = 0.
EN_PIO2	6	PIO2 input when EN_PIO2 = 0.
EN_PIO3	7	PIO3 input when EN_PIO3 = 0.
RD	8	Bidirectional.
EN_SZ_RD	9	RD, SIZ[0-2] inputs when EN_SZ_RD = 0.
BR*	10	3-state output.
ACK[0-2]*	11-13	Bidirectional.
EN_ACK	14	ACK[0-2]* inputs when EN_ACK = 0.
SIZ[0-2]	15-17	Bidirectional.
D[0-31]	18-49	Bidirectional.
EN_DATA	50	D[0-31] inputs when EN_DATA = 0.
PA[2-7]	51-56	Input.
SCLK	57	Input.
LERR*	58	Input.
OE	59	Input.
AS*	60	Input.
BG*	61	Input.
SEL*	62	Input.
RESET*	63	Input.
INTR*	64	Open-drain output.
EN_INTR*	65	INTR* 3-state when EN_INTR* = 1.

Name	BS Reg Bit #	Description
ENPUR	66	Input.
TO	67	3-state output.
CHIDX	68	Bidirectional.
EN_CHIDX	69	CHIDX input when CHIDX = 0.
CHIDR	70	Bidirectional.
EN_CHIDR	71	CHIDR input when CHIDR = 0.
CHICK	72	Bidirectional.
CHIFS	73	Bidirectional.
EN_CHI	74	CHICK and CHIFS inputs when EN_CHI = 0.
CKCOD	75	3-state output.
FSCOD	76	3-state output.
RCLK	77	Input.
TECK	78	3-state output.
EN_MISC	79	TECK, CKCOD, FSCOD, BR*, and TO 3-state when EN_MISC = 0.
NTPR	80	Input: (NTRPR), ignore.
NTNR	81	Input: (NTRNR), ignore.
NTPT	82	Output: (NTPIP).
NTNT	83	Bidirectional, input in EXTEST (NTNSNS).
TENT	84	Bidirectional, input in EXTEST (TENSNS).
TEPT	85	Output: (TEPIP).
TEPR	86	Input: (TERPR), ignore.
TENR	87	Input: (TERNR), ignore.

SBus Operation

Transfer Modes Supported

In master mode, the DBRI supports 16-, 8-, 4-, and 1-word transfers. It does not support 16-bit or 8-bit transfers, or 2-word transfers. If a 16-word transfer fails, an 8-word transfer is tried. If an 8-word transfer fails, a 4-word transfer is tried. If a 4-word transfer fails, a 1-word transfer is tried. If a 4- or 8-word transfer succeeds after a longer block transfer fails, then no longer length transfers are tried. REG0 bits S and E provide a software reset mechanism for this feature. In slave mode, the DBRI only supports 1-word transfers. It responds to an 8- or 16-bit read request with word acknowledge. It responds to an 8- or 16-bit write request with error acknowledge.

FCode

Approximately 100 system clock cycles after the rising edge of the RESET* (soft reset also), 48 bytes of FCode are available at locations 0 to 47 in the physical address space. They can be read after this, but cannot be written. If the host attempts to read FCode before it is ready, the DBRI does not respond until it is ready (IDL/WAIT ACK). When it is ready, it responds with WORD ACK and the FCode is presented on the SBus. They are available via an SBus slave mode read until REG8 is written. If the code is accessed via 8- or 16-bit read requests, the FCode is presented on the SBus as a 32-bit word, containing 4 bytes of FCode. Since PA0 and PA1 are not on the DBRI, PA2-PA7 determine which 4-byte group of FCode bytes are read.

The FCode provided by Sun for the current silicon is as follows: (hex) `fd 00 09 ea 00 00 00 30 12 0a 53 55 4e 57 2c 44 42 52 49 65 01 14 12 04 6e 61 6d 65 01 10 01 02 a5 a6 7d 1e 01 03 a6 80 01 16 a8 63 a5 01 17 00`.

Error Handling in the Slave Mode

The DBRI (in slave mode) always responds to a word transfer with a word acknowledge. If the FCode is accessed by byte or half-word requests, the DBRI responds with a word acknowledge, and 32-bit word is available at the SBus. If the DBRI receives slave write requests (the CPU or other masters write into the DBRI internal registers) with transfer size other than a word, it responds with error acknowledges. The DBRI responds with error acknowledge to any burst transfer request. The DBRI also responds with error acknowledge to any attempts to access the empty locations. Any attempts to write to the registers which contain FCode also receives error acknowledge.

The DBRI in the slave mode does not respond with any acknowledge but a word, error, or idle acknowledge. This imples the LateError* (LERR*) signal never be driven in the slave mode. Therefore, the LERR* pin is an input only and not a bidirectional pin.

Error Handling in the Master Mode

Rerun Acknowledge

The DBRI in master mode repeats the bus cycle when it detects the rerun acknowledge. If the DBRI detects the rerun acknowledge in a single-word cycle, it repeats the cycle. It releases the bus, requests the bus, and transfers the data when the bus is granted. If the DBRI detects the rerun acknowledge at the beginning of a burst mode transfer, it terminates the current cycle and repeats the cycle including the bus request. As specificed in the SBus specification, the rerun acknowledge can be only the first acknowledge for the bus burst cycle. Therefore, the DBRI checks this rerun acknowledge only for the first data word. But if the DBRI ever detects the rerun acknowledge in the middle of burst transfer, it simply terminates the current cycle and repeats the cycle including the bus request.

Be aware that the DBRI does not take any action when an infinite number of rerun acknowledges are received in the same transaction other than repeating the same cycle as long as it receives the rerun acknowledge. Note that the multiple rerun acknowledges do not cause any interrupts.

Error Acknowledge

The DBRI repeats the cycle if it detects the error acknowledge in single-word transfers. The DBRI terminates the current cycle and repeats the entire cycle including the bus request if it detects error acknowledge in the middle of burst mode transfer.

The error acknowledge is handled the same way as the rerun acknowledge except that the error acknowledge can be detected in the middle of burst transfers.

Late Error

The DBRI completes the current cycle and repeats the entire cycle if it detects the LateError* whether it is a single-word transfer or burst transfer.

During a retry of the cycle due to the late error, if the DBRI detects the LateError* again, it completes the current cycle, sets the MLE bit in REG1, disables the master mode (sets the D bit in REG0), and generates an interrupt at the end of the cycle.

The DBRI does not attempt to discard the data or rewrite the data when it detects the LateError*, but simply repeats the cycle because it is too late by the time the DBRI detects this condition.

Lost Bus Grant

If the bus grant is taken away in the middle of bus transfer for any reason, the DBRI terminates the current cycle to give up the bus and generates an interrupt without writing in the interrupt queue. The DBRI does not repeat the cycle. The DBRI does not take any actions other than this interrupt. The LBG bit (bit 2) in REG1 is set.

Multiple Errors Burst Mode Transfers

The DBRI tries a shorter burst mode if it detects the error acknowledge (not the rerun acknowledge, not the LateError*) for the first word in the burst transfer. For example, if the DBRI detects the error acknowledge in an 8-word burst transfer, it tries 4-word burst transfers (there are two 4-word burst transfers if the G bit in REG0 is enabled). Unless the DBRI detects the error acknowledge in 4-word burst transfers, the 4-word burst remains the longest burst transfer. The DBRI tries single-word transfers if it detects the error acknowledge in 4-word burst transfers.

If the DBRI starts with 16-word burst transfer, this process continues until the DBRI tries single-word transfers if it detects the error acknowledge for the first word of the burst transfers in the next shorter burst transfers.

In order to go back to the longer burst modes, the S, E, or G bit in REG0 must be set. See descriptions below for the details.

Error Acknowledge in 16-Word Burst Transfer

If 16-word bursts are enabled (S bit in REG0 is set):

During first attempt of each transaction:

If the Error Ack is received after the first Word Ack, then retry the 16-word burst transaction once, and only once.

If Error Ack is the first word response, disabled 16-word burst (unset bit S in REG0 and remain disabled until REG0 is rewritten by the host), set the MBE bit in REG1, generate an interrupt, and then attempt next smaller transaction size (8-word burst if E bit in REG0 is set, 4-word burst if E bit in REG0 is not set but G bit in REG0 is set).

During retry of 16-word burst:

If the Error Ack is received after the first Word Ack, the DBRI terminates the transaction, sets the MRR bit, generates an interrupt, and responds as described below.

The DBRI sets the D bit in REG0, which disables master mode activity. Master mode I/O remains disabled until the DBRI is reset or until the host clears the D bit by writing to REG0.

Note: This does not disable the 16-word burst mode.

If Error Ack is the first word response, disable 16-word burst (clear S bit in REG0 and remain disabled until REG0 is rewritten by host), set the MBE bit in REG1, generate an interrupt, and then attempt next smaller transaction size (8-word burst if E bit in REG0 is set, 4-word burst if E bit in REG0 is not set but G bit in REG0 is set).

Error Acknowledge in 8-Word Burst Transfer

If 8-word bursts are enabled (E bit in REG0 is set):

During first attempt of each transaction:

If the Error Ack is received after the first Word Ack, then retry the 8-word burst transaction once, and only once.

If Error Ack is the first word response, disable 8-word burst (clear E bit in REG0 and remain disabled until REG0 is rewritten by host), set the MBE bit in REG1, generate an interrupt, and then attempt next smaller transaction size (4-word burst if G bit in REG0 is set, single-word if G bit is not set).

During retry of 8-word burst:

If the Error Ack is received after the first Word Ack, the DBRI terminates the transaction, sets the MRR bit, generates an interrupt, and responds as described below.

The DBRI sets the D bit in REG0, which disables the master mode activity. Master mode I/O remains disabled until the DBRI is reset or until the host clears the D bit by writing to REG0.

Note: This does not disable the 8-word burst mode.

If Error Ack is the first word response, disable 8-word burst (clear E bit in REG0 and remain disabled until REG0 is rewritten by host), set the MBE bit in REG1, generate an interrupt, and then attempt next smaller transaction size (4-word burst if G bit in REG0 is set, single-word if G bit is not set).

Error Acknowledge in 4-Word Burst Transfer

If 4-word bursts are enabled (G bit in REG0 is set):

During first attempt of each transaction:

If the Error Ack is received after the first Word Ack, then retry the 4-word burst transaction once, and only once.

If Error Ack is the first word response, disable 4-word burst (clear G bit in REG0 and remain disabled until REG0 is rewritten by host or reset by hardware or software reset), set the MBE bit in REG1, generate an interrupt, and then attempt next smaller transaction size (1 word).

During retry of 4-word burst:

If the Error Ack is received after the first Word Ack, the DBRI terminates the transaction, sets the MRR bit, generates an interrupt, and responds as in section E.

The DBRI sets the D bit in REG0, which disables master mode activity. Master mode I/O remains disabled until the DBRI is reset or until the host clears the D bit by writing to REG0.

Note: This does not disable the 4-word burst mode.

If Error Ack is the first word response, disable 4-word burst (clear G bit in REG0 and remain disabled until REG0 is rewritten by host or reset by hardware or software reset), set the MBE bit in REG1, generate an interrupt, then attempt next smaller transaction size (1 word).

Multiple Errors in Single-Word Transfers

On a 1-word transaction: If an Error Ack is received, DBRI retries the transaction once, and only once.

On retry of 1-word transaction:

If the Error Ack is received, the DBRI terminates the transaction, sets the MRR bit, generates an interrupt, and responds as described below.

The DBRI sets the D bit in REG0, which disables the master mode activity. Master mode I/O remains disabled until the DBRI is reset or until the host clears the D bit by writing to REG0.

I/O Specifications

Clock Inputs

Any input which serves to clock storage elements or latch other inputs is a clock input. Rise and fall times are specified at 10%-90% points.

Other Inputs

The setup and hold time specifications are the minimum durations of an input signal respectively before and after the clock edge latching of a particular input signal. These are expressed in terms of 50% transition points.

Outputs

The reference signal is the external input which initiates the transition of the specified output.

Propagation delay is generally measured from the 50% point of the reference signal transition to the 50% point of the output signal transition.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Min	Typ	Max	Unit
Ambient Operating Temperature	0	-	70	°C
Storage Temperature	-40	-	150	°C
Voltage on Any Pin with Respect to Ground (Vss)	-0.25	-	V_{DD} +0.25	V
Power Dissipation	-	-	1.25	W

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 ohms, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 40. ESD Threshold Voltage

Device	Voltage
T7259-FC	500 V

Electrical Characteristics

Ambient temperature = 0 °C to 70 °C, V_{DD} = 5.0 V ± 5%, Vss = 0.0 V (unless otherwise specified).

Table 41. Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Nom	Max	Unit
Input Voltage:						
Low	V_{IL}	-	-0.5	-	0.8	V
High	V_{IH}	-	2.4	-	V_{DD} + 0.25	V
Output Voltage:		SBus Outputs				
Low	V_{OL}	I_{OL} = 10 mA	-	-	0.4	V
High	V_{OH}	I_{OH} = -10 mA	2.8	-	-	V
Input Leakage Current:						
TTL Inputs	I_{ILH}, I_{ILL}	V_{IH} = 5.25 V	-	-	10	µA
Inputs with Pull-Up	I_{ILHP}, I_{ILLP}	V_{IH} = 5.0 V	-	-	500	µA
Power Supply Current f_{SCLK} = 25 MHz, C_L = 100 pF	I_{DDM}	0 °C, V_{DD} = 5.25 V	-	80	95	mA
Power Dissipation	PD_1	25 °C, V_{DD} = 5.0 V	-	389	450	mW
f_{SCLK} = 25 MHz, C_L = 100 pF	PD_2	70 °C, V_{DD} = 5.25 V	-	-	500	mW